STUDENT HAND BOOK

2023-24

(3-2)

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Vision of the Institute

To be recognized as a premier institution in offering the value based and futuristic quality technical education to meet the technological need of the society.

Mission of the the Institute

- To impart value quality technical education through innovative teaching and learning methods.
- To continuously produce employable technical graduates with advanced technical skills to meet the current and future technological need of the society.
- To prepare the graduate for high learning with emphasis on academic and industrial research

Vision of the Department

To promote excellence in technical education and scientific research in electronics and communication engineering for the benefit of society.

Mission of the Department

- To impart excellent technical education with state of art facilities inculcating values and lifelong learning attitude.
- To develop core competence in our students imbibing professional ethics and team spirit.
- To encourage research benefiting society through higher learning

PEOs:

PEO 1: Establish themselves as successful professionals in their career and higher education in the field of Electronics & Communication Engineering and allied domains through rigorous quality education.

PEO 2: Develop Professionalism, Ethical values, Excellent Leadership qualities, Communication Skills and teamwork in their Professional front and adapt to current trends by engaging in lifelong learning

PEO 3: Apply the acquired knowledge & skills to develop novel technology and products for solving real life problems those are economically feasible and socially relevant

PEO 4: To prepare the graduates for developing administrative acumen, to adapt diversified and multidisciplinary platforms to compete globally.

Quality Policy

Our quality policy is to continuously strive for over-all development of the department and the students. Our policy is to provide best inputs to the students and to develop them to imbibe the spirit of professionalism, dedication & commitment.

Dress Code

We encourage our students to be formally dressed on and off campus. This nurtures the feeling of equality and belongings among the students fraternity.

All students are required to carry Photo Identity card at all the time while in the campus

POs:

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions.(WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health,

safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, andas a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for

i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

PSOs:

- Ability to apply concepts of Electronics & Communication Engineering to associated research areas of electronics, communication, signal processing, VLSI, Embedded systems
- Ability to design, analyze and simulate a variety of Electronics & Communication functional elements using hardware and software tools along with analytic skills

A Bird's Eye view about the Institution

CMR Engineering College, popularly known as CMREC is the brain child of the clairvoyant CH.Narasihma Reddy. CMR Engineering College is one of the best engineering Colleges for aspiring engineering students. It is one of the newly established Colleges by CMR Engineering Educational Society. CMR Engineering College was established in 2010 in 10 Acres and built up area of 4,785.78 Sq.m. with a single - minded aim to provide a perfect platform to students in the field of Engineering, Technology for their academic and overall personality development. The college has a very good academic activity which focuses for the campus placement.

The college is approved by the All India Council for Technical Education, New Delhi and is affiliated to JNT University Hyderabad. The CMREC is offering the three under graduate courses in ECE, CSE and MECH, and post graduate course in ECE and CSE.

Today, CMREC has grown in leaps and bounds and it is no wonder that CMREC has become cynosure of the eyes of many, hankering for the distinguished centre of technologicallearning.

Discipline, Character and Education are the three tenets for which CMREC stands, is certainly the haven where values blend seamlessly to churn out engineers for future.

- Collaborating with Institutions and Industries.
- Promoting research and development programme for the growth of economy.
- Disseminating technical knowledge in the region by continuing education programmes.
- Aiming at continual improvement of all round development of student

Department Profile

The Department of Electronics and Communication engineering of CMR Engineering College was established in the academic year 2010-11 with an annual intake of 120.The intake was increased to 180 from the academic year 2012-13 and later the intake was increased to 240 from the academic year 2013-14. In addition to this intake, the Department has 20% lateral entry students at II B.Tech level.

M.Tech programme was started with 24 intake in the specialization of Embedded Systems from the year 2013-14 and VLSI System Design from the year 2014-15.

The B.Tech (ECE) program is duly approved by the AICTE and Government of Telangana and affiliated to Jawaharlal Nehru Technological University (JNTUH),Hyderabad. Three batches have graduated so far.

Department have 56 faculty and are members of professional bodies like ISTE,IEEE,IETE. Some of the students are the members of IETE student forum and IEEE student branch of the existing Department. A technical association (ECMRON) of ECE has been formed by the senior students of the department for the benefits of students to impart additional knowledge in the field of E&C Engineering apart from prescribed curriculum.

The Department has well equipped state of art laboratories to gain good knowledge and technical skills in the field of Electronics, Communication, Microwave, VLSI, Digital Signal Processing & Microprocessors & Microcontrollers. The Department periodically organizes seminars, symposia, workshops and guest lectures for the benefit of both the students and the faculty.

Established: 2010 EAMCET Code: CMRN

Academic Regulations, Course Structure and Detailed Syllabus under Autonomous Status

BACHELOR OF TECHNOLOGY (B.TECH.)

(CMREC – R-20 Regulations)

(Applicable for the batch admitted from 2020-2021)

PRELIMINARY DEFINITIONS AND NOMENCLATURES

AICTE: Means All India Council for Technical Education, New Delhi.

Autonomous Institute: Means an institute designated as Autonomous by University Grants Commission (UGC), New Delhi in concurrence with affiliating University (Jawaharlal Nehru Technological University, Hyderabad) and State Government of Telangana.

Academic Autonomy: Means freedom to an institute in all aspects of conducting its academic programs, granted by UGC for Promoting Excellence.

Academic Council: The Academic Council is the highest academic body of the institute and is responsible for the maintenance of standards of instruction, education and examination within the institute. Academic Council is an authority as per UGC regulations and it has the right to take decisions on all academic matters including academic research.

Academic Year: It is the period necessary to complete an actual course of study within a year. It comprises two main semesters i.e., (one odd + one even) and supplementary semester.

Branch: Means specialization in a program like B.Tech. degree program in Electronics and communication Engineering, B.Tech degree program in Computer Science and Engineering, etc.

Board of Studies (BOS): BOS is an authority as defined in UGC regulations, constituted by Head of the Organization for each of the departments separately. They are responsible for curriculum design and updation in respect of all the programs offered by a department.

Backlog Course: A course is considered to be a backlog course, if the student has obtained a failure grade (F) in that course.

Basic Sciences: The courses offered in the areas of Mathematics, Physics, Chemistry etc., are considered to be foundational in nature.

Commission: Means University Grants Commission (UGC), New Delhi.

Choice Based Credit System: The credit based semester system is one which provides flexibility in designing curriculum and assigning credits based on the course content and hours of teaching along with provision of choice for the student in the course selection.

Compulsory course: Course required to be undertaken for the award of the degree as per the program.

Continuous Internal Examination: It is an examination conducted towards sessional assessment.

Core: The courses that are essential constituents of each engineering discipline are categorized as professional core courses for that discipline.

Course: A course is a subject offered by a department for learning in a particular semester.

Course Outcomes: The essential skills that need to be acquired by every student through a course.

Credit: A credit is a unit that gives weight to the value, level or time requirements of an academic course. The number of 'Contact Hours' in a week of a particular course determines its credit value. One credit is equivalent to one lecture/tutorial/lab hour per week.

Credit point: It is the product of grade point and number of credits for a course.

Cumulative Grade Point Average (CGPA): It is a measure of cumulative performance of a student over all the completed semesters. The CGPA is the ratio of total credit points secured by a student in various courses in all semesters and the sum of the total credits of all courses in all the semesters. It is expressed up to two decimal places.

Curriculum: Curriculum incorporates the planned interaction of students with instructional content, materials, resources, and processes for evaluating the attainment of Program Educational Objectives.

Department: An academic entity that conducts relevant curricular and co-curricular activities, involving both teaching and non-teaching staff, and other resources in the process of study for a degree.

Dropping from Semester: Student who does not want to register for any semester can apply in writing in prescribed format before the commencement of that semester.

Elective Course: A course that can be chosen from a set of courses. An elective can be Professional Elective and or Open Elective.

Evaluation: Evaluation is the process of judging the academic performance of the student in her/his courses. It is done through a combination of continuous internal assessment and semester end examinations.

Grade: It is an index of the performance of the students in a said course. Grades are indicated by alphabets.

Grade Point: It is a numerical weight allotted to each letter grade on a 10 - point scale.

Honors: An Honors degree typically refers to a higher level of academic achievement at an undergraduate level.

Institute: Means CMR Engineering, Hyderabad unless indicated otherwise by the context.

Massive Open Online Courses (MOOC): MOOC courses inculcate the habit of self- learning. MOOC courses would be additional choices in all the elective group courses.

Minor: Minor are coherent sequences of courses which may be taken in addition to the courses required for the B.Tech. degree.

Pre-requisite: A specific course or subject, the knowledge of which is required to complete before student register another course at the next grade level.

Professional Elective: It indicates a course that is discipline centric. An appropriate choice of minimum number of such electives as specified in the program will lead to a degree with specialization.

Program: Means, UG degree program: Bachelor of Technology (B.Tech.) and PG degree program: Master of Technology (M.Tech.).

Program Educational Objectives: The broad career, professional and personal goals that every student will achieve through a strategic and sequential action plan.

Project work: It is a design or research based work to be taken up by a student during his/her final year to achieve a particular aim. It is a credit based course and is to be planned carefully by the student.

Re-Appearing: A student can reappear only in the semester end examination for theory component of a course, subject to the regulations contained herein.

Registration: Process of enrolling into a set of courses in a semester of a program.

Regulations: The regulations, common to all B.Tech. programs offered by Institute, are designated as – CMREC Regulations – R-20 and are binding on all the stakeholders.

Semester: It is a period of study consisting of 15 to 18 weeks of academic work equivalent to normally 90 working days. Odd semester commences usually in July and even semester in December of every year.

Semester End Examinations: It is an examination conducted for all courses offered in a semester at the end of the semester.

Student Outcomes: The essential skill sets that need to be acquired by every student during her/his program of study. These skill sets are in the areas of employability, entrepreneurial, social and behavioral.

University: Means Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, is an affiliating University.

Withdraw from a Course: Withdrawing from a course means that a student can drop from a course within the first two weeks of odd or even semester. However, he / she can choose a substitute course in place of it by exercising the option within 5 working days from the date of withdrawal.

FOREWORD

The autonomy is conferred to CMR Engineering College (CMREC), Hyderabad by University Grants Commission (UGC), New Delhi based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies including JNT University Hyderabad (JNTUH), Hyderabad and AICTE, New Delhi. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf. Thus, an autonomous institution is given the freedom to have its own examination system and monitoring mechanism, independent of the affiliating University but under its observance.

CMREC is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies such as Academic Council and Board of Studies (BOS) are constituted with the guidance of the Governing Body of the institute and recommendations of the JNTUH to frame the regulations, course structure, and syllabi under autonomous status.

The autonomous regulations, course structure, and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the institute in order to produce a quality engineering graduate to the society.

All the faculty, parents, and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and from the principal of the institute, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is requested for the successful implementation of the autonomous system in the larger interests of the institute and brighter prospects of engineering graduates.

PRINCIPAL

ACADEMIC REGULATIONS FOR B.TECH. REGULAR STUDENTS WITH EFFECT FROM ACADEMIC YEAR 2020 – 21 (CMREC R-20)

For pursuing four year under graduate Bachelor Degree Programme of study in Engineering (B.Tech.) offered by CMR Engineering College under Autonomous status is here in referred to as CMREC (An Autonomous Institution)

All the rules specified here in approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2020-21 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for CMR Engineering College (An Autonomous Institution).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, CMR Engineering College shall be the chairman Academic Council.

1.0 Under-Graduate Degree Programme in Engineering & Technology (UGP in E&T)

CMR Engineering College offers a 4-year (8 semesters) Bachelor of Technology (B.Tech.) degree programme, under Choice Based Credit System (CBCS) with effect from the academic year 2020-21.

ADMISSION

Admission first year of four-year B. Tech. Degree Program of study in Engineering

Eligibility

A candidate seeking admission into the first year of four year B. Tech. Degree Program should have:

Passed either Intermediate Public Examination (I.P.E.) conducted by the Board of Intermediate Education, Telangana, with Mathematics, Physics and Chemistry as optional subjects or any equivalent examination recognized by Board of Intermediate Education, Telangana or a Diploma in Engineering in the relevant branch conducted by the Board of Technical Education, Telangana or equivalent Diploma recognized by Board of Technical Education for admission as per guidelines defined by the Regulatory bodies of Telangana State Council for Higher Education (TSCHE) and AICTE.

Secured a rank in the EAMCET examination conducted by the Telangana State Government or on the university or in the basis of any other order of merit approved by the university, for allotment of a seat by the Convener, EAMCET.

Admission Procedure

Admissions are made into the first year of four year B. Tech. Degree Program as per the stipulations of the TSCHE.

Category A seats are filled by the Convener, TSEAMCET (70%).

Category B seats are filled by the Management (30%).

Admission into the second year of four year B. Tech. degree Program in Engineering

Eligibility

A candidate seeking admission under lateral entry into the II year I Semester B. Tech. degree Program should have passed the qualifying exam (B.Sc. Mathematics or Diploma in concerned course) and based on the rank secured by the candidate in Engineering Common Entrance Test ECET (FDH) in accordance with the instructions received from the Convener, ECET and Government of Telangana allotted the seats.

Admission Procedure

Admissions are made into the II year of four year B. Tech. Degree Program through Convener, ECET (FDH) against the sanctioned strength in each Program of study as lateral entry students.

B. TECH. PROGRAMME STRUCTURE

Programs Offered

CMR Engineering College, an autonomous institution affiliated to JNTUH, offers the following B. Tech. Programs of study leading to the award of B. Tech. degree under the autonomous scheme.

B.Tech. Computer Science and Engineering

B.Tech. Computer Science and Engineering (Artificial Intelligence & Machine Learning)

B.Tech. Computer Science and Engineering (Data Science)

B.Tech. Computer Science and Engineering (Cyber Security)

B.Tech. Electronics and Communication Engineering

B.Tech. Information Technology

B.Tech. Mechanical Engineering

Duration of the Programs

A student after securing admission shall complete the B.Tech. programme in a minimum period of four academic years (8 semesters), and a maximum period of eight academic years (16 semesters) starting from the date of commencement of first year first semester, failing which student shall forfeit seat in B.Tech. course. Each student shall secure 160 credits (with CGPA ≥ 5) required for the completion of the under graduate programme and award of the B.Tech. Degree.

UGC / AICTE specified definitions / descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations / norms, which are listed below.

Semester Scheme

Each under graduate programme is of 4 academic years (8 semesters) with the academic year divided into two semesters of 22 weeks (□90 instructional days) each, each semester having - Continuous Internal Evaluation (CIE) and Semester End Examination (SEE).

Credit Courses

All subjects / courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject / course in an L: T: P: C (lecture periods: tutorial periods: practical periods: credits) structure based on the following general pattern.

One credit for one hour / week / semester for theory / lecture (L) courses or Tutorials.

One credit for two hours / week / semester for laboratory / practical (P) courses. Courses like Environmental Science, Constitution of India, Intellectual Property Rights, and Gender Sensitization lab are mandatory courses. These courses will not carry any credits.

Subject Course Classification

All subjects / courses offered for the under graduate program in E&T (B. Tech. degree programs) are broadly classified as follows.

S. No.	Broad Course Classification	Course Group / Category	Course Description
1	Foundation Courses (FnC)	BS – Basic Sciences	Includes mathematics, physics and chemistry subjects
2		ES - Engineering Sciences	Includes fundamental engineering subjects
3		HS – Humanities and Social sciences	Includes subjects related to humanities, social sciences and management
4	Core Courses (CoC)	PC – Professional Core	Includes core subjects related to the parent Discipline / department / branch of Engineering
5	Elective Courses (EℓC)	PE – Professional Electives	Includes elective subjects related to the parent Discipline / department / branch of Engineering.
6		OE – Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline / department / branch of Engineering.
7	Core Courses	Project Work	B.Tech. project or UG project or UG major project or Project Stage I & II
8		Industrial training / Mini- project	Industrial training / Summer Internship / Industrial Oriented Mini-project /Mini-project
9		Seminar	Seminar / Colloquium based on core contents related to parent discipline / department / branch of Engineering.
10		-	Mandatory courses (non-credit)

COURSE REGISTRATION

A faculty advisor or counselor shall be assigned to a group of 20 students, who will advise the students about the under graduate programme, its course structure and curriculum, choice / option for subjects / courses, based on their competence, progress, pre-requisites and interest.

The academic section of the college invites “registration forms” from students before the beginning of the semester through “on-line registration”, ensuring “date and time of starting”. The on-line registration requests for any “current semester” shall be completed before the commencement of SEEs (Semester End Examinations) of the ‘preceding semester’.

A student can apply for on-line registration, only after obtaining the ‘written approval’ from faculty advisor / counselor, which should be submitted to the college academic section through the Head of the Department. A copy of it shall be retained with Head of the Department, faculty advisor / counselor and the student.

If the student submits ambiguous choices or multiple options or erroneous entries during on-line registration for the subject(s) / course(s) under a given / specified course group / category as listed in the course structure, only the first mentioned subject / course in that category will be taken into consideration.

Subject / course options exercised through on-line registration are final and cannot be changed or inter-changed further and alternate choices also will not be considered. However, if the subject / course that has already been listed for registration by the Head of the Department in a semester could not be offered due to any unforeseen or unexpected reasons, then the student shall be allowed to have alternate choice either for a new subject (subject to offering of such a subject), or for another existing subject (subject to availability of seats). Such alternate arrangements will be made by the head of the department, with due notification and time-framed schedule, within the first week after the commencement of class-work for that semester.

Dropping of subjects / courses may be permitted, only after obtaining prior approval from the faculty advisor/ counselor with in a period of 15days “from the beginning of the current semester”.

Open Elective Course: Students can choose One Open Elective Course (OEC-I) during VI Semester, one (OEC-II) during VII Semester and one (OEC-III) in VIII Semester from the list of Open Elective Courses given. However, Students cannot op for an Open Elective Courses offered by their own (parent) Department, if it is there in the already listed under any category of the Subjects offered by parent Department in any Semester.

Professional Electives: The students have to choose six professional electives (PE-I to PE-VI) from the list of professional electives.

SUBJECTS / COURSES TO BE OFFERED

A typical section (or class) strength for each semester shall be 60.

A subject / course may be offered to the students, only if a minimum of 20 students (1/3 of the section strength) opt for it. The maximum strength of a section is limited to 80 (60 + 1/3 of the section strength).

More than one faculty member may offer the same subject (lab / practical may be included with the corresponding theory subject in the same semester) in any semester. However, selection of choice for students will be based on – "first come first serve basis and CGPA criterion" (i.e., the first focus shall be on early on-line entry from the student for registration in that semester, and the second focus, if needed, will be on CGPA of the student).

If more entries for registration of a subject comes into picture, then the Head of the Department concerned shall decide, whether or not to offer such a subject / course for two (or more) sections.

In case of options coming from students of other departments / branches / disciplines (not considering open electives), first priority shall be given to the student of the "Parent Department".

ATTENDANCE REQUIREMENTS

A student shall be eligible to appear for the semester end examinations, if the student acquires a minimum of 75% of attendance in aggregate of all the subjects / courses (excluding attendance in mandatory courses like Environmental Science, Constitution of India, Intellectual Property Rights, and Gender Sensitization lab) for that semester. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. This attendance should be included in the fortnight attendance.

The attendance of Mandatory Non-Credit courses should be uploaded separately.

Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned by the college academic committee on genuine and valid grounds, based on the students representation with supporting evidence.

A stipulated fee shall be payable for condoning of shortage of attendance.

Shortage of attendance below 65% in aggregate shall in no case be condoned.

Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester. They get detained and their registration for that semester shall stand cancelled. They will not be promoted to the next semester. They may seek re-registration for all those subjects registered in that semester, in which the student is detained, by seeking re-admission into that semester as and when offered; if there are any professional electives and / or open electives, the same may also be re-registered if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the same set of elective subjects offered under that category.

A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same class.

ACADEMIC REQUIREMENTS

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no. 6.0.

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject / course, if student secures not less than 35% (25 marks out of 70 marks) in the semester end examination, and a minimum of 40% (40 marks out of 100 marks) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of letter grades, this implies securing "C" grade or above in that subject / course.

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Industrial Oriented Mini Project / Summer Internship and seminar, if the student secures not less than 40% marks (i.e., 40 out of 100 allotted marks) in each of them. The student is deemed to have failed, if he/she (i) does not submit a report on Industrial Oriented Mini Project / Summer Internship, or does not make a presentation of the same before the evaluation committee as per schedule, or (ii) does not present the seminar as required in the IV year I Semester, or (iii) secures less than 40% marks in Industrial Oriented Mini Project / Summer Internship and seminar evaluations.

A student may reappear once for each of the above evaluations, when they are scheduled again; if the student fails in such "one reappearance" evaluation also, the student has to reappear for the same in the next subsequent semester, as and when it is scheduled.

Promotion Rules

S. No.	Promotion	Conditions to be fulfilled
1	First year first semester to first year second semester	Regular course of study of first year first semester.
2	First year second semester to second year first semester	(i) Regular course of study of first year second semester.
		(ii) Must have secured at least 19 credits out of 39 credits i.e., 50% credits up to first year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
3	Second year first semester to second year second semester	Regular course of study of second year first semester.
4	Second year second semester to third year first semester	Regular course of study of second year second semester. Must have secured at least 47 credits out of 79 credits i.e., 60% credits up to second year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
5	Third year first semester to third year second semester	Regular course of study of third year first semester.
6	Third year second semester to fourth year first semester	Regular course of study of third year second semester. Must have secured at least 71 credits

		out of 119 credits i.e., 60% credits up to third year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
7	Fourth year first semester to fourth year second semester	Regular course of study of fourth year first semester.

A student (i) shall register for all courses / subjects covering 160 credits as specified and listed in the course structure, (ii) fulfils all the attendance and academic requirements for 160 credits, (iii) earn all 160 credits by securing SGPA > 5.0 (in each semester), and CGPA (at the end of each successive semester) >5.0, (iv) passes all the mandatory courses, to successfully complete the under graduate program. The performance of the student in these 160 credits shall be taken into account for the calculation of "the final CGPA" (at the end of under graduate program), and shall be indicated in the grade card of IV year II semester

If a student registers for "extra subjects" (in the parent department or other departments / branches of Engg.) other than those listed subjects totaling to 160 credits as specified in the course structure of his / her department, the performances in those "extra subjects" (although evaluated and graded using the same procedure as that of the required 160 credits) will not be taken into account while calculating the SGPA and CGPA. For such 'extra subjects' registered, percentage of marks and letter grade alone will be indicated in the grade card as a performance measure, subject to completion of the attendance and academic requirements as stated in regulations 6.0 and 7.1 – 7.4 above.

A student eligible to appear in the semester end examination for any subject / course, but absent from it or failed (thereby failing to secure "C" grade or above) may reappear for that subject / course in the supplementary examination as and when conducted. In such cases, internal marks (CIE) assessed earlier for that subject / course will be carried over, and added to the marks to be obtained in the SEE supplementary examination for evaluating performance in that subject.

A student detained in a semester due to shortage of attendance may be re-admitted in the same semester in the next academic year for fulfillment of academic requirements. The academic regulations under which a student has been readmitted shall be applicable. However, no grade allotments or SGPA / CGPA calculations will be done for the entire semester in which the student has been detained.

A student detained due to lack of credits, shall be promoted to the next academic year only after acquiring the required academic credits. The academic regulations under which the student has been readmitted shall be applicable to him / her.

EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of a student in every subject / course (including practical and Project Stage – I & II) will be evaluated for 100 marks each, with 30 marks allotted for CIE (Continuous Internal Evaluation) and 70 marks for SEE (Semester End-Examination).

For all Theory Courses as mentioned above, the distribution shall be 30 marks for CIE, and 70 marks for the SEE.

For Theory Subjects

Continuous Internal Evaluation (CIE)

During the Semester, there will be two mid-terms examinations for 30 marks each. Each mid-term examination consists of one subjective paper for 25 marks and assignment for 5 marks for each subject.

Question paper contains two Parts (Part-A and Part-B). The distribution of marks for PART- A and PART-B will be 10 marks & 15 marks respectively for UG programs.

Pattern of the question paper is as follows.

PART–A

Consists of Five Short answer Questions each carrying two mark. The I-Mid-term examination shall be conducted for the 50% of the syllabus and II-Mid-term examination shall be conducted for remaining 50% of the syllabus.

PART-B

Consists of Three questions (out of which students have to answer three questions) carrying five marks each. Each question there will be an “either” “or” choice (that means there will be two questions from each unit and the student should answer any one question). The questions may consist of sub-questions also.

The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus.

First Assignment should be submitted before the commencement of the first mid-term examinations, and the Second Assignment should be submitted before the commencement of the second mid-term examinations. The assignments shall be specified / given by the concerned subject teacher.

The total marks secured by the student in each mid-term examination are evaluated for 30 marks, and the average of the two mid - term examinations shall be taken as the final marks secured by each student in Continuous Internal Evaluation.

If any student is absent for any subject of Mid-term examination, an online test (CBT - Computer Based Test) will be conducted for him / her by the institute.

Semester End Examination (SEE)

The Semester End Examination (SEE) will be conducted for 70 marks consisting of Two parts i). Part - A for 20 marks ii). Part - B for 50 marks.

Part - A is compulsory question consisting of ten sub-questions. Two sub-questions from each unit and carry 2 marks each.

Part - B consist of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these questions is from one unit may contain sub-questions. For each question there will be "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.

For Practical Courses

Continuous Internal Evaluation (CIE)

There shall be a Continuous Internal Evaluation (CIE) during the Semester for 30 marks with a distribution of 20 marks for day-to-day evaluation and10 marks for internal lab exam. One internal practical test shall be conducted by the concerned laboratory teacher.

Semester End Examination (SEE)

SEE shall be conducted for 70 marks with an external examiner and the laboratory teacher concerned. The external examiner shall be appointed by the Chief Controller of Examinations of the college. The external examiner should be selected from the outside college among the autonomous / reputed institutions from a panel of three examiners submitted by the concerned BOS Chairman of the Department.

Engineering Graphics

For the Subjects having Design and / or Drawing, (such as Engineering Graphics, Engineering Drawing, Machine Drawing, Production Drawing Practice, and Estimation), the distribution shall be 30 marks for CIE (20 marks for day-to-day work and timely submission of drawing sheets and 10 marks for internal tests). There shall be two internal tests in a semester and the average of the two shall be considered for the award of marks for CIE.

The distribution of marks for SEE shall be 70 marks. SEE shall consist of five questions carrying 14 marks each. Each of these questions is from one unit and may contain sub - questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.

There shall be an Internship / Mini Project, in collaboration with an industry of their specialization. Students will register for this immediately after III year II semester (VI Semester) end examinations and pursue it during summer vacation. The evaluation of Mini project will be done at the end of IV Year I semester (VII semester). It shall be evaluated internally for 100 marks. The committee consisting of Project Coordinator, Supervisor of the project and one senior faculty of the department will evaluate the mini Project and award appropriate Grade, based on the report submitted to the department and presentation provided by the student in front of the committee.

Major Project - It shall be carried out in two stages

Project Stage – I shall be evaluated internally during IV Year I Semester, Project Stage – II shall be evaluated externally during IV Year II Semester. Each stage will be evaluated for 100 marks. Student has to submit project work report at the end of each semester. First report includes project work carried out in IV Year I semester and second report include project work carried out in IV Year I & II Semesters. SEE for both project stages shall be completed before the commencement of SEE Theory examinations.

For Project Stage – I, the departmental committee consisting of Head of the Department, project supervisor and a senior faculty member shall evaluate the project work for 70marks and project supervisor shall evaluate for 30 marks. Two reviews shall be conducted. Review-I will be conducted within a month from the commencement of class work (problem definition, objective, literature survey) and Review-II will be conducted before second mid examination (brief description and sample case study, progress of work, presentation and report submission). Average of the two reviews will be taken for 100 marks.

The student is deemed to have failed, if he (i) does not submit a report on Project Stage

- I or does not make a presentation of the same before the evaluation committee as per schedule, or (ii) secures less than 40% marks. A student who has failed may reappear once for the above evaluation, when it is scheduled again; if he fails in such “one reappearance” evaluation also, he has to reappear for the same in the subsequent

semesters, as and when it is scheduled. The topics for industrial oriented mini project, seminar and Project Stage – I shall be different from one another.

Project Stage – II is the continuation of Project Stage – I. It shall be evaluated by the external examiner for 70 marks and the project supervisor shall evaluate it for 30 marks. Two reviews should be conducted. Review-I will be conducted within a month from the commencement of class work (progress of work, discussion and presentation) and Review- II will be conducted before second mid examination (progress of work, results, discussion, presentation and report submission). Average of the two reviews will be taken for CIE. The Project Viva-voce (SEE) shall be conducted by a committee comprising of an External Examiner, Head of the Department and Project Supervisor. In SEE marks, 20% for working model / simulation / data collection, 20% for report preparation and 60% for presentation and viva-voce. The external examiner should be selected by Chief Controller of Examinations / Principal from outside the college among the autonomous / reputed institutions from a panel of three examiners submitted by the concerned Head of the Department.

The student is deemed to have failed, if he / she (i) does not submit a report on Project Stage II, or does not make a presentation of the same before the external examiner as per schedule, or (ii) secures less than 40% marks in the sum total of the CIE and SEE taken together. A student who has failed may reappear once for the above evaluation, when it is scheduled again; if student fails in such "one reappearance" evaluation also, he / she has to reappear for the same in the next subsequent semester, as and when it is scheduled.

Seminar

For Seminar presentation, the student shall collect the information on a specialized topic, prepare a Technical Report and submit to the department at the time of seminar presentation. The seminar presentation (along with the technical report) shall be evaluated by a committee consisting of Seminar coordinator and two senior faculty members with appropriate grade. The seminar report shall be evaluated internally for 100 marks. There shall be no semester end examination for the seminar.

Mandatory Non-Credit Courses

Mandatory Non-Credit Courses offered in any semester, a "Satisfactory / Not Satisfactory" shall be awarded to the student based on the performance in both CIE and SEE.

AWARD OF GRADES

Grades will be awarded to indicate the performance of students in each theory subject, laboratory / practicals, seminar, Industry Oriented Mini Project, and project Stage - I & II. Based on the percentage of marks obtained (Continuous Internal Evaluation plus Semester End Examination, both taken together) as specified in item 8.0 above, a corresponding letter grade shall be given.

As a measure of the performance of a student, a 10-point absolute grading system using the following letter grades (as per UGC / AICTE guidelines) and corresponding percentage of marks shall be followed.

% of Marks Secured in a Subject/Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
Greater than or equal to 90%	O (Outstanding)	10
80 and less than 90%	A+ (Excellent)	9
70 and less than 80%	A (Very Good	8
60 and less than 70%	B+ (Good)	7
50 and less than 60%	B (Average)	6
40 and less than 50%	C (Pass)	5
Below 40%	F (FAIL)	0
Absent	Absent	0

A student who has obtained an "F" grade in any subject shall be deemed to have "failed" and is required to reappear as a "supplementary student" in the semester end examination, as and when offered. In such cases, internal marks in those subjects will remain the same as those obtained earlier.

To a student who has not appeared for an examination in any subject, "Absent" grade will be allocated in that subject, and he / she is deemed to have "failed". A student will be required to reappear as a "supplementary student" in the semester end examination, as and when offered next. In this case also, the internal marks in those subjects will remain the same as those obtained earlier.

A letter grade does not indicate any specific percentage of marks secured by the student, but it indicates only the range of percentage of marks.

A student earns grade point (GP) in each subject / course, on the basis of the letter grade secured in that subject / course. The corresponding "credit points" (CP) are computed by multiplying the grade point with credits for that particular subject / course.

Credit points (CP) = grade point (GP) x credits …. For a course

A student passes the subject / course only when GP > 5 ("C" grade or above)

The Semester Grade Point Average (SGPA) is calculated by dividing the sum of credit points (∑CP) secured from all subjects / courses registered in a semester, by the total number of credits registered during that semester. SGPA is rounded off to two decimal places. SGPA is thus computed

For each semester,

where “i” is the subject indicator index (takes into account all subjects in a semester), “N” is the number of subjects “registered” for the semester (as specifically required and listed under the

course structure of the parent department), Ci is the number of credits allotted to the ith subject, and Gi represents the grade points (GP) corresponding to the letter grade awarded for that ith subject.

The Cumulative G*j*ra=**1**de Point Average (CGPA) is a measure of the overall cumulative performance of a student in all semesters considered for registration. The CGPA is the ratio of the total credit points secured by a student in all registered courses in all semesters, and the total number of credits registered in all the semesters. CGPA is rounded off to two decimal places. CGPA is thus computed from the I year II semester onwards at the end of each semester as per the formula

Course / Subject	Credits	Letter Grad
Course 1	4	A
Course 2	4	O
Course 3	4	C
Course 4	3	B
Course 5	3	A+
Course 6	3	C
	21	

CGPA = 518 / 69 = 7.51

The above illustrated calculation process of CGPA will be followed for each subsequent semester until VIII semester. The CGPA obtained at the end of VIII semester will be the final CGPA secured for entire B. Tech. Program for the student.

For merit ranking or comparison purposes or any other listing, only the "rounded off"

values of the CGPA's will be used.

SGPA and CGPA of a semester will be mentioned in the semester Memorandum of Grades if all subjects of that semester are passed in first attempt. Otherwise the SGPA and CGPA shall be mentioned only on the Memorandum of Grades in which sitting he / she passed his

/ her last exam in that semester. However, mandatory courses will not be taken into consideration.

PASSING STANDARDS

A student shall be declared successful or "passed" in a semester, if he / she secures a GP ≥ 5.00 ("C" grade or above) in every subject / course in that semester (i.e., when the student gets an SGPA

> 5.00 at the end of that particular semester); and he shall be declared successful or "passed" in the entire under graduate program, only when gets a CGPA > 5.00 for the award of the degree as required.

After the completion of each semester, a grade card or grade sheet shall be issued to all the registered students of that semester, indicating the letter grades and credits earned. It will show the details of the courses registered (course code, title, number of credits, grade earned, etc.), credits earned.

Declaration of results

Computation of SGPA and CGPA are done using the procedure listed in 9.6 to 9.9.

For final percentage of marks equivalent to the computed final CGPA, the following formula may be used.

% of Marks = (final CGPA – 0.5) x 10

AWARD OF DEGREE

A student who registers for all the specified subjects / courses as listed in the course structure and secures the required number of 160 credits (with CGPA > 5.0), within 8 academic years from the date of commencement of the first academic year, shall be declared to have "qualified" for the award of B.Tech. Degree in the chosen branch of Engineering selected at the time of admission.

A student who qualifies for the award of the degree as listed in item 12.1 shall be placed in the following classes.

Class Awarded	CGPA to be Secured	
First Class with distinction	≥ 7.50	From the CGPA secured from 160 Credits
First Class	≥ 6.50 and < 7.50	
Second Class	≥ 5.50 and < 6.50	
Pass Class	≥ 5.00 and < 5.50	
Fail	< 5.00	

WITHHOLDING OF RESULTS

If the student has not paid the tuition fees to the institution at any stage, or has dues pending due to any reason whatsoever, or if any case of indiscipline is pending, the result of the student may be withheld, and the student will not be allowed to go into the next higher semester. The award or issue of the degree may also be withheld in such cases.

STUDENT TRANSFERS

There shall be no branch transfers after the completion of admission process.

Transfer candidates (from non-autonomous college affiliated to JNTUH): A student who is following JNTUH curriculum, transferred from other college to this institute in third semester or subsequent semesters shall join with the autonomous batch in the appropriate semester. Such candidates shall be required to pass in all the courses in the program prescribed by the Board of Studies concerned for that batch of students from that semester onwards to be eligible for the award of degree. However, exemption will be given in the courses of the semester(s) of the batch which he / she had passed earlier and substitute courses are offered in their place as decided by the Board of Studies. The student has to clear all his backlog courses up to previous semester by appearing for the supplementary examinations conducted by JNTUH for the award of degree. The total number of credits to be secured for the award of the degree will be the sum of the credits up to the previous semester under JNTUH regulations and the credits prescribed for the semester in which a candidate joined after transfer and subsequent semesters under the autonomous status. The class will be awarded based on the academic performance of a student in the autonomous pattern.

ACADEMIC REGULATIONS FOR B.TECH. (LATERAL ENTRY SCHEME) FROM THE ACADEMIC YEAR 2021 – 22

Eligibility for award of B. Tech. Degree (LES)

The LES students after securing admission shall pursue a course of study for not less than three academic years and not more than six academic years.

The student shall register for 121 credits and secure 121 credits with CGPA ≥ 5 from II year to IV year B.Tech. programme (LES) for the award of B.Tech. degree.

The students, who fail to fulfill the requirement for the award of the degree in six academic years from the year of admission, shall forfeit their seat in B.Tech.

The attendance requirements of B.Tech. (Regular) shall be applicable to B.Tech. (LES).

Promotion Rule

S. No	Promotion	Conditions to be fulfilled
1	Second year first semester to second year second semester	Regular course of study of second year first semester.
2	Second year second semester to third year first semester	Regular course of study of second year second semester. Must have secured at least 24 credits out of 40 credits i.e., 60% credits up to second year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
3	Third year first semester to third year second semester	Regular course of study of third year first semester.

4	Third year second semester	Regular course of study of third year second semester. Must have secured at least 48 credits out of 80 credits i.e., 60% credits up to third year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
5	Fourth year first semester to fourth year second semester	Regular course of study of fourth year first semester.

All the other regulations as applicable to B. Tech. 4-year degree course (Regular) will hold good for B. Tech. (Lateral Entry Scheme).

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

S. No	Nature of Malpractices / Improper conduct	Punishment
	If the student	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which student is appearing but has not made use of (material shall include any marks on the body of the student which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical)	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester.

		The hall ticket of the student is to be cancelled and sent to the University.

3	Impersonates any other student in connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semesters. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with For feature of seat.

5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the chief superintendent/ assistant superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination cancellation of their performance in subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The students also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the Course by the student is subject to the

		academic regulations in connection with forfeiture of seat.
8	Possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The student is also debarred and forfeits the seat.
9	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The student is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared for including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester.
	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the student has appeared for including practical examinations and project work of that

11		semester examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award a suitable punishment.	

Transfer candidates (from an autonomous college affiliated to JNTUH): A student who has secured the required credits up to previous semesters as per the regulations of other autonomous institutions shall also be permitted to be transferred to this institute. A student who is transferred from the other autonomous colleges to this institute in third semester or subsequent semesters shall join with the autonomous batch in the appropriate semester. Such candidates shall be required to pass in all the courses in the program prescribed by the Board of Studies concerned for that batch of students from that semester onwards to be eligible for the award of degree. However, exemption will be given in the courses of the semester(s) of the batch which he / she had passed earlier and substitute subjects are offered in their place as decided by the Board of Studies. The total number of credits to be secured for the award of the degree will be the sum of the credits up to previous semester as per the regulations of the college from which he / she is transferred and the credits prescribed for the semester in which a candidate joined after transfer and subsequent semesters under the autonomous status. The class will be awarded based on the academic performance of a student in the autonomous pattern.

SCOPE

The academic regulations should be read as a whole, for the purpose of any interpretation.

In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Council is final.

Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

ACADEMIC CALENDAR (2023-24)

CMR ENGINEERING COLLEGE

UGC AUTONOMOUS

(Approved by AICTE - New Delhi. Affiliated to JNTUH and Accredited by NAAC & NBA)
Kandlakoya (V), Medchal (M), Medchal - Malkajgiri (D)-501401

ACADEMIC CALENDAR (REVISED)
B.Tech III-YEAR: ACADEMIC YEAR (2023-24)

III B.Tech. I – SEMISTER

S. No.	EVENT	DATE		DURATION
		FROM	TO	
1	Commencement of Class Work	**21.08.2023**		---
2	First Spell of Instructions	21.08.2023	14.10.2023	8 weeks
3	**First Mid Term Examinations (Theory & Practical)**	***16.10.2023***	***21.10.2023***	***1 Week***
4	**Dusara Vacation***	***23.10.2023***	***28.10.2023***	***1 Week***
5	Submission of First Mid Term Marks to Exam Branch	30.10.2023		---
6	Parents Teacher's Meeting	04.11.2023		---
7	Second Spell of Instructions	30.10.2023	23.12.2023	8 weeks
8	**Second Mid Term Examinations (Theory & Practical)**	***26.12.2023***	***30.12.2023***	***1 Week***
9	Submission of Second Mid Term Marks to Exam Branch	06.01.2024		---
10	Preparation Holidays and Practical Examinations	01.01.2024	06.01.2024	1 week
11	**End Semester & Supplementary Examinations**	***08.01.2024***	***20.01.2024***	***2 Weeks***

III B.Tech. II – Semester

S. No.	EVENT	DATE		DURATION
		FROM	TO	
1	Commencement of II-SEM Class work	**29.01.2024**		---
2	First Spell of Instructions	29.01.2024	23.03.2024	8 weeks
3	**First Mid Term Examinations**	***26.03.2024***	***30.03.2024***	1 week
4	Submission of First Mid Term Marks to Exam Branch	06.04.2024		---
5	Parents Teacher's Meeting	13.04.2024		
6	Second Spell of Instructions	01.04.2024	11.05.2024	6 weeks
7	**Summer Vacation**	***13.05.2024***	***25.05.2024***	2 weeks
8	Continuation of Second Spell of Instructions	27.05.2024	08.06.2024	2 weeks
9	**Second Mid Term Examinations**	***10.06.2024***	***15.06.2024***	1 week
10	Submission of Second Mid Term Marks to Exam Branch	22.06.2024		---
11	Preparation Holidays and Practical Examinations	17.06.2024	22.06.2024	1 week
12	**End Semester & Supplementary Examinations**	***24.06.2024***	***06.07.2024***	***2 weeks***
13	Commencement of Class Work for the next A.Y-2024-2025	***08.07.2024***		---

- * **Dusara Vacation** (Subjected to declaration by JNTUH / TS Govt.)

Controller of Examination
CMR Engineering College
(Autonomous)
Kandlakoya (V), Medchal Dist.,
Hyderabad, T.S. - 501 401.

Controller of Examinations

Principal
CMR Engineering College
(Autonomous)
Kandlakoya (V), Medchal Dist.,
Hyderabad, T.S. - 501 401.

Principal

Department event planner (2023-24)

S.NO	DATE	NAMEOFTHEEVENT
1	04/12/2023	Commencement of Class Work for IV Year
2	29/01/2024	Commencement of Class Work for III Year
3	19/02/2024	Commencement of Class Work for II Year
4	04/12/2023- 27/01/2024	I Spell of instructions for IV Year
5	29/01/2024- 23/03/2024	I Spell of instructions for III Year
6	19/02/2024- 13/04/2024	I Spell of instructions for II Year
7	30/12/2024-31/12/24	IV B.Tech Major Project Work Review
9	14/12/2023	Student Workshop-I for III Year
10	15/03/24	Industrial visit
11	10/01/2024- 11/01/2024	IV B.Tech Major Project Work Review II
12	29/01/2024- 31/01/2024	I MID Exams for IV Year
15	07/08/2024	Guest lecture for III year
16	10/02/2024	Submission of I mid marks for IV Years to University
18	26/03/2024- 30/03/2024	IMID Exams for III Year
19	26/03/2024- 30/03/2024	IMID Lab Internal Exam for III Year
21	15/04/2024- 20/04/2024	IMID Exams for II Year
22	15/03/2024- 16/03/2024	IMID Lab Internal Exam for II Year
23	06/04/2024	Submission of I mid marks for III Years to University
24	27/04/2024	Submission of I mid marks for II Years to University
25	06/09/2024	Professional Body Activities
26	01/02/2024- 27/03/2024	II Spell of instructions for IV Years (Including I mid examinations)
27	01/04/2024- 11/05/2024	II Spell of instructions for III Years (Including I mid examinations)

28	22/04/2024- 11/05/2024	II Spell of instructions for II Years(Including I mid examinations)
29	11/03/2024-12/03/24	IV B.Tech Major Project Work Review III
30	28/03/2024- 30/03/2024	II MID Exams for IV Years
31	06/04/2024	Marks Submission of II mid for IV Years to University
32	01/04/2024- 06/04/2024	Preparation and project evaluation
33	08/04/2024- 20/04/2024	End Semester Exams for IV Years
34	12/03/2024	Workshop for II year
35	10/06/2024- 15/06/2024	II MID Exams for III Years
36	01/07/2024- 06/07/2024	II MID Exams for II Years
37	22/06/2024	Marks Submission of II mid for III Years to University
38	13/07/2024	Marks Submission of II mid for II Years to University
39	01/07/2024- 06/07/2024	II Lab Internal Exam for II Year
40	10/06/2024- 13/06/2024	II Lab Internal Exam for III Year
41	06/07/2024- 10/07/2024	Lab External Exam for II Year
42	15/06/2024- 18/06/2024	Lab External Exam for III Year
43	17/06/2024- 22/06/2024	Preparation Holidays and Practical Examinations for III years
44	08/07/2024- 13/07/2024	Preparation Holidays and Practical Examinations for II years
45	24/06/2024- 06/07/2024	End Semester Exams for III Years
46	15/07/2024- 27/07/2024	End Semester Exams for II Years

List of subjects:

S.NO	Course code	Course Title
1	EC601PC	Embedded system design
2	EC602PC	Antennas and Microwave Engineering
3	EC603PC	VLSI Design
4		professional elective-II
5		open elective-1/MOOCS
6	EC604PC	Antennas and Microwave Engineering lab
7	EC605PC	ECAD Lab
8	EC606PC	Embedded system design Lab
9	MC609	Intellectual property rights
10	MC610	Employability Skills-v

CMR Engineering College

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EMBEDDED SYSTEM DESIGN

Subject Code: EC601PC

Class: III Year B. Tech II Semester

BY

K. SUBRAMANYA CHARI
ASSISTANT PROFESSOR

2022-23

S.NO **CONTENT**

(1) - Preamble/Introduction
(2) - Prerequisites
(3) - Objectives and Outcomes
(4) - Syllabus
1. R20-CMREC
2. GATE
3. IES
(5) - List of Expert Details (Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6) - Journals with min 5 ref paper for literature study
(7) - Subject -Lesson plan
(8) - Suggested Books (prescribed and References)
(9) - Websites for self learning Resources like *www.geeksforgeeks.org, www.schools.com, Coursera , edX, Udemy, Khan Academy*, NPTEL etc along Registration procedures*)*
(10) - Question Banks
1. JNTUH/Model papers
2. GATE
(11) - Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications.
(12) - Assignment Question/Innovative Assignments sets.
(13) -List of topics for students Seminars with Guidelines
(14) - STEP/Course material in softcopy
(15) - Expert Lectures with topics & Schedules (if any)

1. **Preamble/Introduction:**

This Subject deals with in detailed study of real time product and project level approach towards the Electronics (appliances, devices, gadgets etc.). Design and development of application based electronic systems with Embedded software at basic and high level coding and merging of multiple software tools. Study about various available processors, controllers, sensors, actuators, memory elements for developing a working model.

2. PREREQUISITES

This subject recommends prior knowledge of basic concepts of Microcontrollers and also Microprocessor and also Embedded fundamentals.

3. OBJECTIVES AND OUTCOMES

COURSE OBJECTIVES

- To provide an overview of Design Principles of Embedded System.
- To provide clear understanding about the role of firmware.
- To understand the necessity of operating systems in correlation with hardware systems.
- To learn the methods of interfacing and synchronization for tasking

COURSE OUTCOMES:

At the end of the course

CO1	Students will be able to **Understand** the selection procedure of processors in the Embedded domain.
CO2	Students will be able to **Design** procedure for Embedded Firmware.
CO3	Students will be able to **Visualize** the role of Real Time Operating Systems in Embedded systems.
CO4	Students will be able to **Evaluate** the correlation between task synchronization and latency issues.

4. SYLLABUS

UNIT 1

Introduction to embedded systems: definition of embedded system, embedded systems Vs general computing systems, history of embedded systems, classification, major application areas, Purpose of embedded systems, characteristics and quality attributes of embedded systems.

UNIT 2

Typical embedded system: core of the embedded system: general purpose and domain specific processors, ASICs, PLDs, commercial-off the shelf components (CTOS), memory: ROM, RAM, memory according to the type of interface, memory shadowing, memory selection for embedded systems, sensors and actuators, communication interface: onboard and external communication interface.

UNIT 3

Embedded firmware: reset circuits, brown-out protection circuits, oscillator unit, real time clock, watchdog timer, embedded firmware design approaches and development languages.

UNIT 4

RTOS based embedded system design: operating system basics, types of operating systems, tasks, process and threads, multiprocessing and multi tasking, task scheduling.

UNIT 5

Task communication: shared memory, message passing, remote procedure call and sockets, task synchronization, task communication, synchronization issues, task synchronization techniques, device drivers, how to choose an RTOS.

Syllabus

(Gate 1-1.5 marks)

Microprocessors, microcontrollers, architecture, shift registers, load and store operations, memories, embedded firmware tools.

Syllabus

(IES)

I/O organization, memory organization, peripheral devices, trends Hardware /software issues Data representation & Programming Operating systems-basics, processes, characteristics, applications Memory management.

5. List of Expert Details

Local:

1. Dr. S. ANURADHA, Assistant Professor, ECE Department, NIT, Warangal.
   E-Mail: anu_praise2004@yahoo.co.in
   Phone No: 8702462446

2. Dr. NARASIMHA RAO BANAVATHU, Assistant Professor, ECE Department, NIT – AP.
   E-Mail: narasimha@nitandhra.ac.in
   Phone: 7989935826

National:

1. Mrs. Chitralekha Mahanta, Ph. D. Professor,
   EEE Department, IIT Guwahati, Guwahati
   Phone: +91 361 2582507 (O), Fax : +91-361-2582542
   email: chitra@iitg.ernet.in
2. Mr. Gupta, Sanjeev, Ph.D. (Communication Engineering),
   Dhirubhai Ambani Institute of Information and Communication, Gandhinagar, Gujrat.
   email: sanjeev_gupta@daiict.ac.in
   Office : (+91) 079-3051-0594
3. Bansal R. K, Ph.D, ECE dept, IIT Kanpur
   Phone: +91-512-2597075, Fax: +91-512-2590063
   Email: rkb@iitk.ac.in

International:

1. Frank Vahid, Professor, Computer Science & Engineering, Univ. of California, Riverside, CA 92521, Office: Winston Chung Hall 328, Lab: WCH 464, (951) 827-4710, vahid@cs.ucr.edu

2. Tony Givargis, Professor of Computer Science University of California, Irvine, Irvine, CA 92697-3435 givargis@uci.edu (949) 824-9357

6. Journals for literature study:

1. Design Automation for Embedded Systems: Springer
   https://www.springer.com/journal/10617

2. International Journal of Embedded Systems: Inderpsace Publishers
   https://www.inderscience.com/jhome.php?jcode=ijes

3. Formation Control of Multiple Mobile Robots Incorporating an Extended State Observer and Distributed Model Predictive Approach | IEEE Journals & Magazine | IEEE Xplore
https://ieeexplore.ieee.org/document/8424483

4. Accelerating Deep Learning Inference in Constrained Embedded Devices Using Hardware Loops and a Dot Product Unit | IEEE Journals & Magazine | IEEE Xplore
https://ieeexplore.ieee.org/document/9187807

5. Embedding Encryption and Machine Learning Intrusion Prevention Systems on Programmable Logic Controllers | IEEE Journals & Magazine | IEEE Xplore
https://ieeexplore.ieee.org/document/8332522

7. Subject - Lesson Plan

S.NO	TOPIC TO BE COVERED	Suggested Books (Eg: T1,T2,R5)	NO. OF LECTURES REQUIRED
UNIT-I Classes required - 11			
1	Introduction: Definition of embedded system,	**T1,R1,R2**	**1**
2	embedded systems Vs general computing systems	**T1,R1,R2,R3**	**1**
3	History of embedded systems	**T1,R1,R2,R3**	**1**
4	Classification of embedded systems,	**T1,R1,R2,R3**	**2**
5	Major application areas	**T1,R1,R2,R3,R4**	**1**
6	Purpose of embedded systems	**T1,R1,R2,R3**	**2**
7	Characteristics of embedded systems	**T1,R1,R2,R3**	**1**
8	Quality attributes of embedded system	**T1**	**2**
UNIT-II Classes required - 10			

9	Typical embedded system: core of the embedded system	**T1,R1,R2**	**1**
10	General purpose and domain specific processors	**T1,R1**	**1**
11	ASICs, PLDs	**T1,R1**	**1**
12	Commercial-off the shelf components (CTOS)	**T1**	**1**
13	Memory: ROM, RAM	**T1,R1,R2**	**1**
14	Memory according to the type of interface	**T1,R2**	**1**
15	Memory shadowing, memory selection for embedded systems	**T1**	**1**
16	Sensors and actuators,	**T1,R1, R2,R3,R4**	**1**
17	Communication interface: onboard communication and external interface.	**T1**	**2**
UNIT-III Classes required - 10			
18	**Embedded firmware:** reset circuits	**T1**	**1**
19	Brown-out protection circuits, oscillator unit	**T1**	**1**
20	Real time clock , watchdog timer	**T1**	**2**
21	Embedded firmware design approaches	**T1,R1,R4**	**3**
22	Embedded development languages.	**T1,R3,R4**	**3**
UNIT-IV Classes required - 10			

23	**RTOS based embedded system design:** operating system basics	**T1,R2,R4**	**3**
24	Types of operating systems, tasks	**T1,R2,R4**	**2**
25	Process and threads, multiprocessing	**T1,R2,R4**	**2**
26	Multitasking, task scheduling.	**T1,R2,R4**	**3**
UNIT-V Classes required - 10			
27	**Task communication:** shared memory,	**T1,R2,R3,R4**	**2**
28	Message passing	**T1,R4**	**1**
29	Remote procedure	**T1,R4**	**1**
30	call and sockets	**T1,R4**	**1**
31	Task synchronization	**T1,R4**	**1**
32	Task communication	**T1,R4**	**1**
33	Synchronization issues	**T1,R4**	**1**
34	Task synchronization techniques,	**T1,R4**	**1**
35	device drivers, how to choose an RTOS	**T1,R4**	**1**
Total No. Classes required 51			

8. Suggested books (Prescribed and references)

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, MC GRAW HILL EDUCATION.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

9. Websites for self learning

1. *https://www.udemy.com/course/introduction-to-embedded-systems-arduino/*
2. *nptel.ac.in/courses/108102045/*
3. *www.nptelvideos.in/2012/11/embedded-systems.html*
4. *users.ece.utexas.edu/valvano/Volume1/E-Book/VideoLinks.html*
5. *https://www.edx.org/course/embedded-systems-shape-the-world-microcontroller-i?index=product&queryID=277d8512fb671362bb57eb84b18ae8c4&position=2*
6. *https://www.youtube.com/watch?v=y9RAhEfLfJs*
7. *https://www.heavy.ai/technical-glossary/embedded-systems*
8. *https://www.coursera.org/articles/embedded-systems*
9. *https://www.oreilly.com/library/view/programming-embedded-systems/0596009836/ch01.html*
10. *https://skill-lync.com/electrical-engineering-courses/fundamentals-embedded-systems*
11. *https://www.edx.org/learn/embedded-systems*

Code No: 137CH **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, December - 2019
EMBEDDED SYSTEM DESIGN
(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Give different classifications of embedded systems.	[2]
b)	GIve the typical characteristics of an embedded system.	[3]
c)	What is the role of DSP in an embedded system design?	[2]
d)	List the differences between RAM and ROM.	[3]
e)	What is an embedded firmware?	[2]
f)	Briefly explain about oscillator unit in Embedded System.	[3]
g)	Write the advantages of threads.	[2]
h)	What is the difference between multiprocessing and multitasking?	[3]
i)	Write the advantages of RPC.	[2]
j)	What is task synchronization in embedded systems?	[3]

PART – B

(50 Marks)

2.	Explain the various purposes of embedded systems in detail with example.	[10]
	OR	
3.	What are the quality attributes of embedded systems? Explain.	[10]
4.	What are the various types of memories used in embedded systems? Explain.	[10]
	OR	
5.	Discuss about external communication interfaces in detail.	[10]
6.	Explain the need of Brown-out Protection Circuit and Watchdog Timer in Embedded System.	[10]
	OR	
7.	What are the different approaches available for Embedded Firmware development?	[10]
8.	Explain how thread and process are used in embedded system.	[10]
	OR	
9.	What are the different types of operating systems? Explain.	[10]
10.a)	Discuss about shared memory in detail.	
b)	Explain Remote Procedure call with an example.	[5+5]
	OR	
11.a)	What is the use of Device Drivers? Explain.	
b)	Discuss about task communication issues in brief.	[4+6]

---ooOoo---

Code No: 117CZ **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, April/May - 2018
EMBEDDED SYSTEM DESIGN
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Give few examples of embedded systems. [2]
b) Give some major applications of Embedded Systems. [3]
c) Write the advantages of PLDs. [2]
d) Explain briefly about memory shadowing. [3]
e) List the types control algorithms design exists in embedded firmware development. [2]
f) What are the circuits are essential for the proper functioning of processor/controller of the embedded system design. [3]
g) What is an operating system? What are its primary functions? [2]
h) What is the use of RTOS in Embedded System Design? [3]
i) Define Coffman conditions. [2]
j) Discuss the issues in Task Synchronization briefly. [3]

PART-B

(50 Marks)

2. Discuss the Characteristics and Quality Attributes of Embedded Systems. [10]

OR

3. Compare the embedded system and general purpose computing system in detail. [10]

4. What is the difference between microprocessors and microcontrollers? Explain the role of microprocessors and controllers in embedded system design. [10]

OR

5. What is sensor? Explain its role in embedded system design. Illustrate with an example. [10]

6. What is the role of reset circuit and Brown-out Protection Circuit in embedded system? [10]

OR

7. Explain the different Embedded Firmware Design Approaches. [10]

8. Explain the different thread binding models for user and kernel level threads. [10]

OR

9. Write the basic design principles when using an RTOS to design of sample RTOS. [10]

10. Explain in detail, the different task communication synchronization issues encountered in Inter Process communication. [10]

OR

11. Explain in detail the following device drivers
a) Serial port device driver.
b) Device drivers for internal programmable timing devices. [5+5]

--ooOoo--

Code No: 117CZ **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, November/December - 2017
EMBEDDED SYSTEM DESIGN
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A
(25 Marks)

1.a)	List the characteristics of an embedded system.	[2]
b)	What is the difference between a system and an embedded system?	[3]
c)	What is actuator?	[2]
d)	What are the considerations for processor selection?	[3]
e)	Explain the role of reset circuit in an embedded system.	[2]
f)	What is the difference between real time clock and watchdog time.	[3]
g)	When do you use cooperative scheduling?	[2]
h)	What is the function of timer in RTOS?	[3]
i)	What is Remote Procedure Call and explain its working?	[2]
j)	What is meant by concurrency of task execution in real time system?	[3]

PART-B
(50 Marks)

2.a) Explain the major application areas of embedded systems.
b) What are the components of Embedded System Hardware? [5+5]

OR

3. Discuss the purpose of embedded systems. List the design metrics used to compare them. [10]

4. With a neat diagram, explain the architecture of a general purpose processor. [10]

OR

5.a) Write the difference between general purpose processors and domain specific processors.
b) Discuss the aspects of memory allocation and mapping in embedded domain. [5+5]

6.a) What are the design criteria of external brown-out protection circuit.
b) How to design and implement firmware for embedded systems? [5+5]

OR

7. Explain with one example, how to change the bus frequency of the processor. [10]

Code No: 137CH **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, March - 2021
EMBEDDED SYSTEM DESIGN
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

- - -

1. What is an embedded system? Explain the different applications of embedded systems. [15]
2. Discuss the Characteristics and Quality Attributes of Embedded Systems. [15]
3. What is Application Specific Integrated Circuited (ASIC)? Explain the role of ASIC in Embedded System Design. [15]
4. Explain on-board and external communication interfaces in detail. [15]
5. What is watchdog timer? Explain its role in embedded system design? [15]
6. What is the role of reset circuit and Brown-out Protection Circuit in embedded system? [15]
7. Explain how 'accurate time management' is achieved in real time kernel. [15]
8. What is device driver? Explain the architecture of device drivers. [15]

---ooOoo---

10. Case study

1. Teaching Hardware/Software Co-design of Embedded Systems – a Case Study

Abstract: To meet the challenges of real embedded development, the students should be trained in applying the hardware/software co-design as a key to ensure a successful final product and to reduce costs and design time. This paper presents a case study describing an undergraduate course project involving design of a simple, but realistic embedded system using hardware/software co-design approach. It demonstrates how Specification and Description Language can be used to model the structure and behavior of the system, as well as to help the partitioning and allocation tasks in the design flow. Conclusions of the impact of using the hardware/software co-design method in the embedded system design projects on raising students' interest and understanding are outlined.

2. Design and development of sensor-based mini projects for embedded system laboratory using ARM Cortex-M3 (LPC1768)

Abstract: In majority of Indian Universities, advanced courses on embedded system design and its related laboratory are not available until the post-graduate level. Early exposure to embedded system design with advanced microcontroller is necessary for computer science and engineering students to face the design challenges in the today's world. This paper presents a mini project-based laboratory for learning embedded system design with different sensors. The aim of this laboratory is to motivate the students to learn the building blocks of embedded systems and control algorithm using the basic hardware and software programming skills provided in this paper, making use of ARM Cortex-M3 processor which is widely used in modern microcontroller products, System on Chip (SoC) and Application Specific Standard Products (ASSP). To enhance the learning process, students are allowed to take this laboratory in three sessions and sensor interfacing projects are provided in the third session. The sensor based projects developed with schematic circuits and software algorithm makes the students to perform all the projects easily and individually. The components including programmer/debugger are inexpensive and can be implemented as take-home projects. It also provides an opportunity to make use as hands-on experience which is then integrated by students to complete their mini project. The feedback from the students shows that most of them were motivated to learn actively all the skills included in the laboratory for embedded system design.

11. Assignment Questions

Unit – 1

1. What are the application areas of embedded systems?
2. Discuss the classifications of embedded systems in detail.
3. Define the purpose of the embedded systems.
4. Describe the characteristics of embedded systems.
5. What are operational and non operational quality attributes of embedded systems?

Unit – 2

1. Discuss about the core of typical embedded system.
2. Differentiate between microprocessor and microcontroller in detail.
3. What are the types of memory elements available for design of embedded systems?
4. Discuss about LED, Switch, Keyboard, Relay, and Opto-coupler in detail.
5. Discuss about Bluetooth, Wi-Fi in detail.

Unit – 3

1. Explain about Reset circuit, Real time clock in detail.
2. Discuss about brown-out protection circuit, Oscillator unit in detail.
3. Define super loop based embedded firmware design approach.
4. Explain embedded OS based embedded firmware design approach.
5. Describe the mixing of high level language with Assembly language.

Unit – 4

1. Discuss the architecture of Operating system with a neat diagram.
2. What are the types of Operating systems available?
3. Define Tasks, Process, Threads, in detail.
4. Discuss about multi-tasking and multi-processing in detail.
5. Describe the process of Task Scheduling in detail.

Unit – 5

1. Discuss the steps involving in task communication in detail.
2. Define shared memory and pipes with case study.
3. Describe message passing, message queue and mail box.
4. Explain any one task synchronization techniques in detail.
5. What are the various device drivers for embedded systems?

12. List of student seminars:

1. Applications of Embedded Systems

2. Classification of Embedded Systems

3. History of Embedded Systems

4. Quality attributes of Embedded Systems

5. Characteristics of Embedded Systems

6. Core of the Embedded Systems

7. PLDs, ASICs, ASSIPs

8. Microprocessor and Microcontrollers

9. Memory and architectures

10. Sensors and actuators

11. Reset Circuit, Brown-out Protection Circuit, Oscillator Unit

12. Real Time Clock, Watchdog Timer

13. Embedded Firmware Design Approaches

14. RTOS Based Embedded System Design

15. Operating System Basics, Types of Operating

16. Systems, Tasks, Process and Threads

17. Multiprocessing and Multitasking, Task Scheduling.

18. Task Communication

19. Shared Memory, Message Passing

20. Remote Procedure Call and

21. Sockets, Task Synchronization

22. Task Communication/Synchronization Issues

23. Task Synchronization Techniques, Device Drivers.

13. Course File
(Attached Separately)

14. Expert Lecture:

S.NO	SUBJECT	TOPIC	YEAR	RESOURCE PERSON	DATE
1	ESD – EL01	Advances in Sensor technology	III-II	Others	30/01/2023
2	ESD - EL02	Working with Wearable devices	III-II	Others	04/03/2023

ACADEMIC PLANNER

SUBJECT: ANTENNA AND WAVE PROPAGATION

S.NO		CONTENT
(1)	-	Preamble/ Introduction
(2)	-	Prerequisites
(3)	-	Objectives and Outcomes
(4)	-	Syllabus
		1.JNTU
		2.GATE
		3.IES
(5)	-	List of Expert Details
(6)	-	Journals
(7)	-	Subject-Lesson Plan
(8)	-	Suggested Books
(9)	-	Websites for Self-Learning
(10)	-	Question Banks
		1.JNTU/Model Papers
		2.GATE
(11)	-	Two Case Study Presentations
(12)	-	Assignment Questions/Innovative Assignments Sets
(13)	-	List of topics for student's seminars
(14)	-	STEP/Course Material
(15)	-	Expert Lectures with Topics & Schedules

(1) *PREAMBLE/ INTRODUCTION*

The tremendous success enjoyed by the cellular phone industry and advances in radio frequency integrated circuits have in recent years fostered the development of various wireless communication systems including near field, indoor and outdoor applications. For aesthetic reasons, all these systems require small antennas that can be embedded into the base station and user equipment's. Furthermore, the development of new services and radio technologies demand for low cost, light weight, miniaturized, efficient antennas for portable wireless devices.

One of the main competencies that a present-day antenna engineer has to possess is the capability to design antennas for portable wireless devices that have good bandwidth, gain and radiation characteristics. This subject is essential to understand the need for designing broadband and miniaturized antennas for wireless applications such as Mobile handsets, Radio frequency identification, Zigbee, Wearable devices and Ultra-wide band communication. This course presents various types of antenna geometry suitable for the above-mentioned wireless devices, the issues in respect of their design and development.

(2) *PREREQUISITES–*

Electromagnetic Field and Waves and Transmission Lines

(3) *OBJECTIVES AND OUTCOMES*

The course objectives are:

1. To understand the concept of radiation, antenna definitions and significance of antennaparameters, to derive and analyze the radiation characteristics of thin wire dipole antennasand solve numerical problems.
2. To analyze the characteristics and design relations of UHF, VHF and Microwave Antennas.
3. To identify the antenna array requirements, to determine the characteristics of ULAs andestimate the patterns of BSA, EFA, and Binomial Arrays.
4. To understand the concepts and set-up requirements for microwave measurements, andfamiliarize with the procedure to enable antenna measurements.
5. To define and distinguish between different phenomenon of wave propagation (ground wave,space wave and sky wave), their frequency dependence, and estimate their characteristics,identifying their profiles and parameters involved.

Upon completing this course, the student will be able to explain the mechanismof radiation, definitions of different antenna characteristic parameters and establish their mathematicalrelations.

1. Characterize the antennas based on frequency, configure the geometry and establish theradiation patterns of VHF, UHF and Microwave antennas and also antenna arrays.
2. Specify the requirements for microwave measurements and arrange a setup to carry out theantenna far zone pattern and gain measurements in the laboratory.

3. Classify the different wave propagation mechanisms, determine the characteristic features ofdifferent wave propagations, and estimate the parameters involved.

(4.1) *SYLLABUS - CMREC*

UNIT - I

Antenna Basics: Basic Antenna Parameters – Patterns, Beam Area, Radiation Intensity, BeamEfficiency, Directivity-Gain-Resolution, Antenna Apertures, Effective Height.

Fields from Oscillating Dipole, Field Zones, Front - to-back Ratio, Antenna Theorems, Radiation,Retarded Potentials – Helmholtz Theorem

Thin Linear Wire Antennas – Radiation from Small Electric Dipole, Quarter Wave Monopole and HalfWave Dipole – Current Distributions, Field Components, Radiated Power, Radiation Resistance, BeamWidth, Directivity, Effective Area and Effective Height, Natural Current Distributions, Far Fields andPatterns of Thin Linear Centre-fed Antennas of Different Lengths. Loop Antennas - Small Loop,Comparison of Far Fields of Small Loop and Short Dipole, Radiation Resistances and Directivities ofSmall Loops (Qualitative Treatment).

UNIT - II

Antenna Arrays: Point Sources – Definition, Patterns**,** arrays of 2 Isotropic Sources **-** Different Cases,Principle of Pattern Multiplication, Uniform Linear Arrays – Broadside Arrays, End fire Arrays, EFA withIncreased Directivity, Derivation of their Characteristics and Comparison, BSAs with Non-uniformAmplitude Distributions – General Considerations and Binomial Arrays.

Antenna Measurements: Introduction, Concepts - Reciprocity, Near and Far Fields, CoordinateSystem, Sources of Errors. Patterns to be Measured, Directivity Measurement, Gain Measurements(by Comparison, Absolute and 3-Antenna Methods)

UNIT - III:

VHF, UHF and Microwave Antennas - I: Arrays with Parasitic Elements, Yagi-Uda Array, FoldedDipoles and their Characteristics, Helical Antennas – Helical Geometry, Helix Modes, Practical DesignConsiderations for Monofilar Helical Antenna in Axial and Normal Modes, Horn Antennas – Types,Fermat's Principle, Optimum Horns, Design Considerations of Pyramidal Horns.

UNIT - IV

VHF, UHF and Microwave Antennas - II: Microstrip Antennas – Introduction, Features, Advantagesand Limitations, Rectangular Patch Antennas – Geometry and Parameters, Characteristics of MicrostripAntennas. Reflector Antennas – Introduction, Flat Sheet and Corner Reflectors, ParaboloidalReflectors – Geometry, Pattern Characteristics, Feed Methods, Reflector Types – Related Features.

UNIT - V:

Wave Propagation - Definitions, Categorizations and General Classifications, Different Modes of WavePropagation, Ray/Mode Concepts,

Ground Wave Propagation –Plane Earth Reflections, Space and Surface Waves, Wave Tilt, CurvedEarth Reflections.

Space Wave Propagation –Field Strength Variation with Distance and Height, Effect of Earth'sCurvature, Absorption, Super Refraction, M-Curves and Duct Propagation, Scattering Phenomena,Troposphere Propagation.

Sky Wave Propagation –Structure of Ionosphere, Refraction and Reflection of Sky Waves byIonosphere, Ray Path, Critical Frequency, MUF, LUF, OF, Virtual Height and Skip Distance, Relationbetween MUF and Skip Distance, Multi-hop Propagation.

(4.2) *SYLLABUS - GATE*

Electromagnetics - Dipole and monopole antennas, linear antenna arrays

SYLLABUS - IES

Electromagnetics - Antennas-radiation pattern, monopoles/dipoles, gain, arrays-active/passive, theory, use.

(5*)* *LIST OF EXPERT DETAILS*

The Expert Details which have been mentioned below are only a few of the eminent ones known Internationally, Nationally and Locally. There are a few others known as well.

INTERNATIONAL

1. **Dr. A. Alphones, Associate Professor, School of Electrical & Electronic Engineering, Nanyang Technological University, Singapore.**
2. **Dr. Gabriel M. Rebeiz, Professor, Electrical and Computer Engineering, University of California, San Diego.**

NATIONAL

1. **Dr. V. Abhai Kumar** – Professor and Director, Thiagarajar College of Engineering, Madurai, Tamil Nadu.
2. **Dr. T. Shanmuganantham**, Associate Professor, Pondicherry University, Pondicherry.

REGIONAL

1. **Dr. Rama Krishna Dasari,** Associate Professor, Osmania University Hyderabad, Telangana.

2. **Dr. Habibulla Khan,** Professor, KL University, Hyderabad, Telangana.

(6) *JOURNALS*

INTERNATIONAL

1. IEEE Transactions on Antennas and Propagation
2. IEEE Antennas and Wireless Propagation Letters
3. IEEE Transaction on Microwave Theory and Techniques
4. IEEE Antenna and Propagation Magazine
5. IET Microwaves, Antennas and Propagation

NATIONAL

1. Journal of Microwave power and Electromagnetic energy
2. Journal of Electromagnetic waves and applications
3. Progress in Electromagnetics Research-PIER
4. Microwave and optical technology letters
5. Electromagnetics

LIST OF REFERENCE PAPERS FOR LITERATURE STUDY

1. **M.A.Jamshed, TimW.C. Brown, F. Heliot, "Antenna Design Consideration for Low SAR mobile terminals", Low Electromagnetic Field Exposure Wireless Device: Fundamentals and Recent Advances, Wiley-IEEE Press, pp: 115-134, 2023,**
2. **G. Muntoni, G. Montisci, A. Melis, M.B. Lodi, N. Cuirreli, M. Simone, "A curved 3D-Printed S-Band patch antenna for plastic cubesat", IEEE Journal of Antenna and Propagation, Vol. 3, pp. 1351-1363, 2022.**
3. **B.G. Parveez Shariff, T.Ali, P.R. Mane, Pradeep kumar, " Array antennas for mmwave applications: A comprehensive review", IEEE Access, Vol.10, pp. 126728-126766, 2022.**

(7) *SUBJECT-LESSON PLAN*

Subject code	Name of the subject	Year/Branch	Name of the Faculty
EC405PC	ANTENNA AND WAVE PROPAGATION	III B.TECH II SEM ECE	Dr. V. Prithivirajan

S.NO	Topic	Sub-Topic	No. of Lectures Required	Suggested Books	Remarks
UNIT – I	Basic Antenna Parameters	Introduction	L1	T1, R1	
		Patters, Beam Area, Radiation Intensity, Beam Efficiency	L2	T1, R1	
		Directivity-Gain Resolution, Antenna Apertures, Effective Height	L3	T1, R1	
		Fields from Oscillating Dipole, Field Zones	L4	T1, R1	
		Front-to-back Ratio, Antenna Theorems, Radiation	L5	T1, R1	
		Retarded Potentials, Helmholtz Theorem	L6	T1, R1	
		Radiation from Small Electric dipole	L7	T1, R1	
		Quarter Wave Monopole and Half Wave Dipole • Current Distribution, • Field Components, • Radiated power, • Radiation	L8, L9	T1, R1	

	Thin Linear Wire Antennas	Resistance, • Beam Width, Directivity • Effective Area, Effective Height			
		Natural Current Distributions, Far Fields Patterns of Thin Linear Centre-fed Antennas of different lengths	L10, L11	T1, R1	
		Loop Antennas • Small Loop, • Comparison of Far Fields of Small Loop and Short Dipole, • Radiation Resistance, Directivities of Small Loops.	L12, L13	T1, R1	
		Problems	L14	T1, R1	
	TOTAL NO OF CLASSES 14				
	Antenna Arrays	Point Sources – Definition, Patterns**,** arrays of 2 Isotropic Sources - Different Cases	L15	T1, R1	
		Principle of Pattern Multiplication	L16	T1, R1	
		Uniform Linear Arrays – Broadside Arrays, End fire Arrays, EFA with Increased Directivity, Derivation of their Characteristics and Comparison	L17, L18, L19	T1, R1	

UNIT – II		BSAs with Non-uniform Amplitude Distributions	L20	T1, R1	
		General Considerations and Binomial Arrays	L21	T1, R1	
	Antenna Measurements	Introduction, Concepts - Reciprocity, Near and Far Fields	L22	T1, R1	
		Coordinate System, Sources of Errors. Patterns to be Measured	L23	T1, R1	
		Directivity Measurement	L24	T1, R1	
		Gain Measurements (by Comparison, Absolute and 3-Antenna Methods)	L25, L26	T1, R1	
	Problems		L27	T1, R1	
	TOTAL NO OF CLASSES 13				
UNIT – III	**VHF, UHF and Microwave Antennas - I**	Arrays with Parasitic Elements	L28	T1, R1	
		Yagi-Uda Array, Folded Dipoles and their Characteristics	L29, L30	T1, R1	
		Helical Antennas – Helical Geometry, Helix Modes, Practical Design Considerations for Monofilar Helical Antenna in Axial and Normal Modes	L31, L32, L33	T1, R1	
		Horn Antennas – Types, Fermat's Principle, Optimum Horns	L34, L35	T1, R1	

		Design Considerations of Pyramidal Horns	L36	T1, R1	
	Problems		L37	T1, R1	
	TOTAL NO OF CLASSES 10				
Unit IV	**VHF, UHF and Microwave Antennas - II**	Microstrip Antennas – Introduction, Features, Advantages and Limitations	L38, L39	T1, R1	
		Rectangular Patch Antennas – Geometry and Parameters	L39, L40	T1, R1	
		Characteristics of Microstrip antennas	L41	T1, R1	
		Reflector Antennas – Introduction, Flat Sheet and Corner Reflectors	L42, L43	T1, R1	
		Paraboloidal Reflectors – Geometry, Pattern Characteristics, Feed Methods	L44, L45	T1, R1	
		Reflector Types – Related Features	L46	T1, R1	
	Problems		L47	T1, R1	
	TOTAL NO OF CLASSES 11				
UNIT –V	**Wave Propagation**	Definitions, Categorizations and General Classifications, Different Modes of Wave Propagation, Ray/Mode Concepts	L48, L49	T2, R2	
	Ground Wave	Plane Earth Reflections, Space and Surface	L50, L51, L52	T2, R2	

	Propagation	Waves, Wave Tilt, Curved Earth Reflections.			
	Space Wave Propagation	Field Strength Variation with Distance and Height, Effect of Earth's Curvature, Absorption, Super Refraction, M-Curves and Duct Propagation, Scattering Phenomena, Troposphere Propagation	L53, L54, L55	T2, R2	
	Sky Wave Propagation	Structure of Ionosphere, Refraction and Reflection of Sky Waves by Ionosphere, Ray Path, Critical Frequency, MUF, LUF, OF, Virtual Height and Skip Distance, Relation between MUF and Skip Distance, Multi-hop Propagation.	L56, L57, L58, L59	T2, R2	
	Problems		L60	T2, R2	
	TOTAL NO OF CLASSES 13				
TOTAL NO OF CLASSES 61					

(8) *SUGGESTED BOOKS*

TEXTBOOKS:

1. Antennas and Wave Propagation – J.D. Kraus, R.J. Marhefka and Ahmad S. Khan, TMH, New Delhi, 4th ed., (Special Indian Edition), 2010.
2. Electromagnetic Waves and Radiating Systems – E.C. Jordan and K.G. Balmain, PHI, 2nd ed. 2000.

REFERENCES:

1. Antenna Theory - C.A. Balanis, John Wiley & Sons, 3rd Ed., 2005.
2. Antennas and Wave Propagation – K.D. Prasad, Satya Prakashan, Tech India Publications, New Delhi, 2001.
3. Radio Engineering Handbook- Keith henney, 3rd edition TMH.
4. Antenna Engineering Handbook –John Leonidas Volakis, 3rd edition, 2007

(9) *WEBSITESFOR SELF LEARNING*

1. The Antenna Theory Website (antenna-theory.com)
2. Microwaves101 | Antenna Design
3. Antenna Designs – Practical Antennas
4. NPTEL - NPTEL :: Electrical Engineering - NOC:Antennas
5. YouTube Channel - (5) Tensorbundle - YouTube

(10.1) *QUESTION BANKS - JNTU*

Drive link
https://drive.google.com/drive/folders/1RCTrDeewONWOKgZxwQ645yk8aw1Qf_UG?usp=share_link

(11) *CASE STUDY PRESENTATIONS*

1. SPECIFIC ABSORPTION RATE

The specific absorption rate (SAR) is a measurement used for determining the amount of radiation absorbed by human tissue when exposed to a radio frequency (RF) electromagnetic field. What's referred to as the *SAR value* is a common property used for measuring absorbed energy, and this value is calculated as:

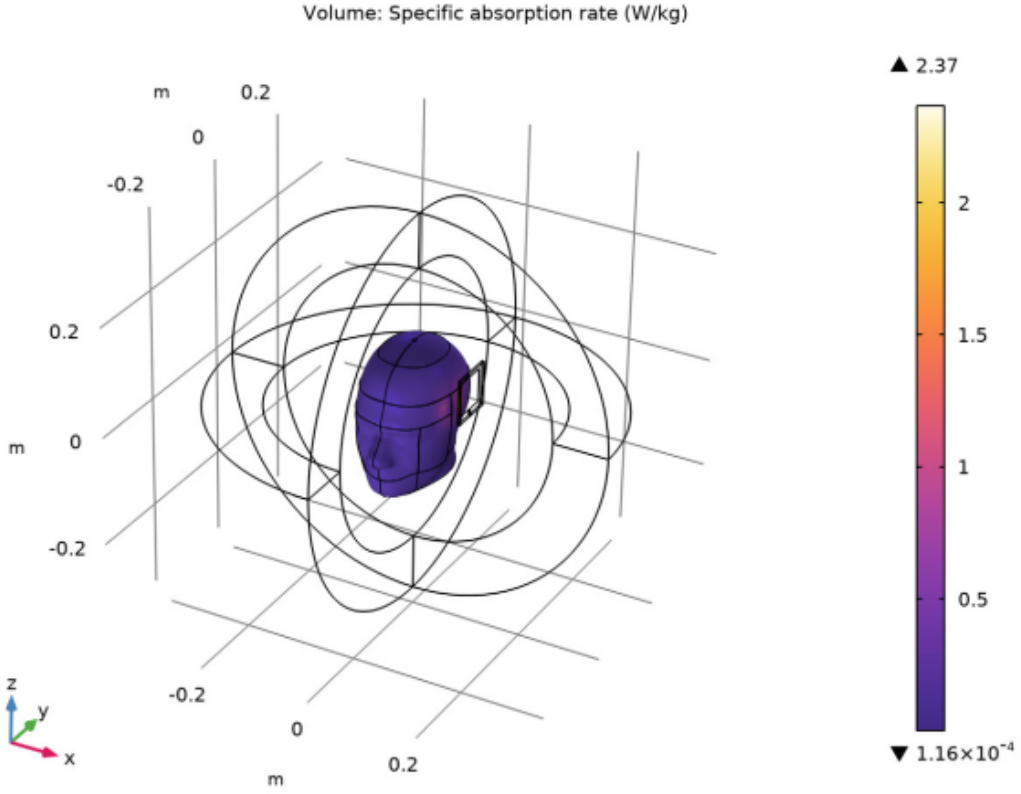
$$E_{\mathrm{SAR}} = \sigma \frac{|\mathbf{E}|^2}{\rho}$$

Here, σ is the human brain tissue's conductivity, ρ is the density, while the norm of the electric field is represented by $|\mathbf{E}|$.

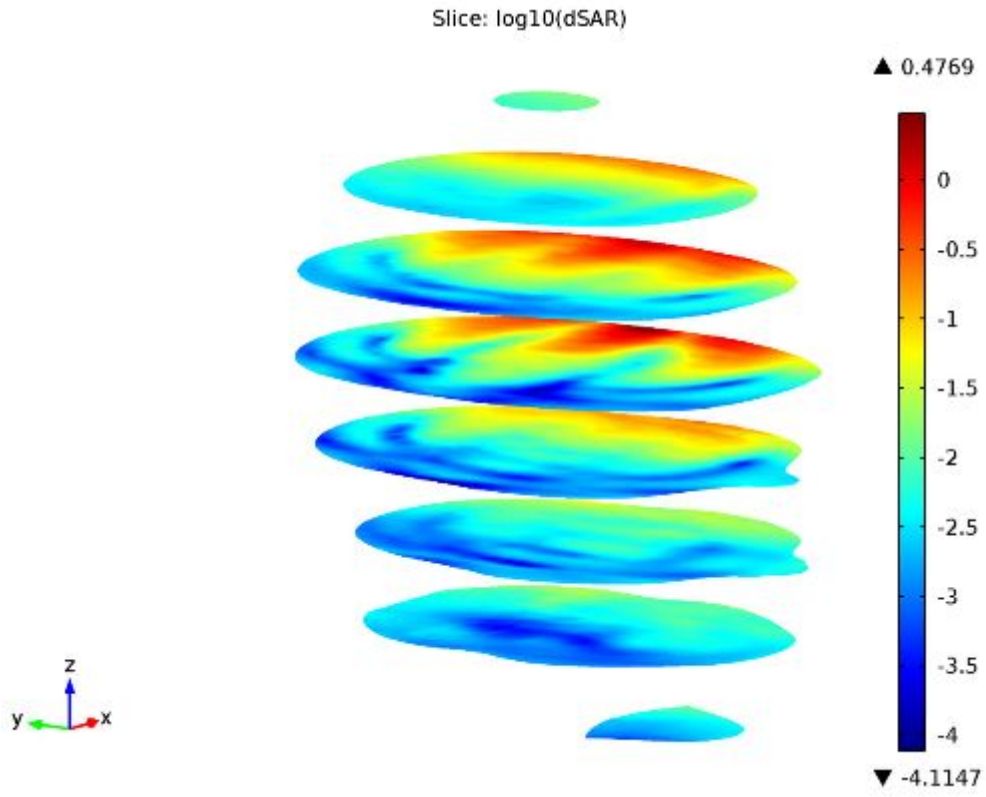
The SAR is typically averaged over the entire body or a smaller sample volume of 10 or 1 g of tissue (which one of these sizes the sample is depends on national rules).

Modeling Local SAR Value in the Human Brain

Human Model has designed using COMSOL Multiphysics.



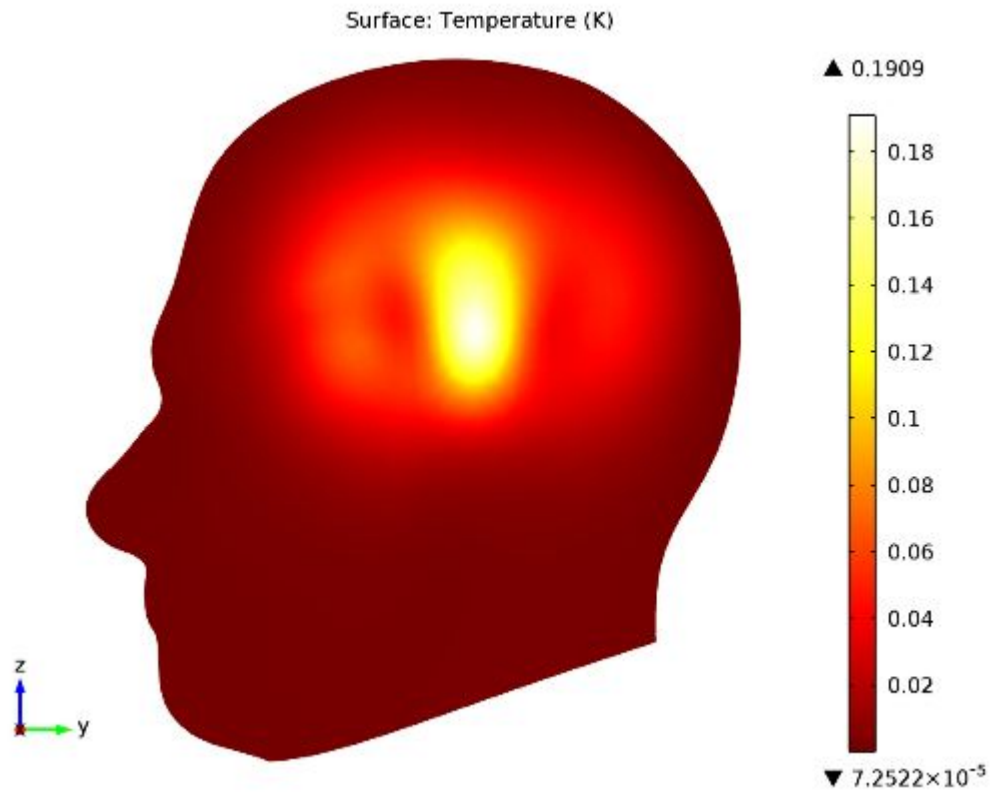
Assuming the radiation is at a frequency of 835 MHz, we can visualize the local SAR value with a log-scale slice plot:



Plot showing local SAR value in the brain tissue.

As you can see above, the SAR value is highest near the head's surface, where it faces the incident wave. You can also notice the difference in electrical properties via the colors in the log-scale plot.

Next, let's tackle the temperature aspect of our problem. For this, we will need to use the bioheat equation, which takes heat loss due to blood flow into account. Intuitively, if we plot this, the temperature is highest near the antenna. The brain tissue temperature increases by under 0.2°C (shown in K in the surface plot below), and drops quickly once inside the head.



Local increase in temperature just under the cell phone antenna.

(12) *ASSIGNMENT QUESTION/ INNOVATIVE ASSIGNMENTSETS*

SET-1

1. Define following with appropriate equation and diagram related to it
   a) Radiation Pattern b) Beam Area c) Directivity d) Aperture area e) Effective height.
2. Derive far field equations of short dipole.
3. Explain the n- array source with equal amplitude and same phase
4. With neat sketch explain basic set up and requirements, for antenna pattern measurement
5. (a)Derive far field equations of Half Wave dipole and also find out Radiation Resistance.
   (b) Derive the directivity of Half wave dipole

SET-2

1. Define following with appropriate expressions and figures.
   a) Radiation Pattern b) Beam Width c) radiation intensity d) antenna aperture e) Effectiveheight
2. Explain the 2-point source with equal amplitude and same phase
3. Calculate radiation resistance of half wave dipole.
4. With neat sketch explain basic set up and requirements, for Directivity measurement
5. (a)Derive far field equations of Quarter Wave mono pole and also find out Radiation Resistance.

(b) Derive the directivity of Half wave dipole

SET-3

1. Calculate radiation resistance of short dipole
2. Explain the n- array source with equal amplitude and different phase
3. Define following with appropriate expressions and figures.
   a) Pattern b) beam area c) radiation intensity d) antenna aperture e) Effective height
4. With neat sketch explain basic set up and requirements, for antenna pattern measurement
5. (a)Derive far field equations of Half Wave dipole and also find out Radiation Resistance.

(b) Derive the directivity of Half wave dipole

(13) *LIST OF TOPICS FOR STUDENT'S SEMINARS*

1. SAR analysis of antenna
2. Smart antenna and its applications
3. Wearable Antennas
4. Impact of Electromagnetic radiation
5. Planar Inverted F-Antenna

(14) *STEP/COURSE MATERIAL*

https://drive.google.com/drive/folders/1RCTrDeewONWOKgZxwQ645yk8aw1Of_UG?usp=share_link

(15) *EXPERT LECTURES WITH TOPICS & SCHEDULES*

1. Guest lecture on "Antenna and Wave Propagation" tentatively scheduled in the month of Feb 2023.

□□□□***THE END*** □□□

ACADEMIC PLANNER
Subject: VLSI DESIGN

S.NO **CONTENT**

(1) - Preamble/Introduction
(2) - Prerequisites
(3) - Objectives and Outcomes
(4) - Syllabus
1.JNTU/R20-CMREC
2.GATE
3.IES
(5) - List of Expert Details(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6) - Journals with min 5 ref paper for literature study
(7) - Subject -Lesson plan
(8) - Suggested Books (prescribed and References)
(9) - Websites for self learning Resources like *www.geeksforgeeks.org, www.schools.com, Coursera,edX, Udemy, Khan Academy*, NPTEL etc along Registration procedures*)*
(10) - Question Banks
1.JNTUH/Model papers
2.GATE
(11) - Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications. **(12) - Assignment Question/Innovative Assignments sets.**
(13) -List of topics for students Seminars with Guidelines
(14) - STEP/Course material in softcopy
(15) - Expert Lectures with topics & Schedules(if any)

(1) - Preamble/Introduction:

VLSI design course gives the knowledge about the fabrication of NMOS, PMOS, CMOS and their application in the present electronics world. The present course gives knowledge about different processes used for fabrication of an IC. The electrical properties of MOS transistor and analysis of CMOS, Bi-CMOS inverters is carried out**.** This course gives detail study on design rules, stick diagrams, logic gates, types of delays, fan-in, fan-out which effects the action of a MOS. It also gives information on data path subsystem and array subsystems, and several PLD's like PLA, PAL, CPLD and FPGA's. We also came to know about the CMOS testing principles both at system level and chip level.

(2) - Prerequisites:

This subject needs the knowledge of basic semiconductor physics, concepts of MOS transistors which are covered in Electronic Devices and Circuits (EDC), digital logic fundamentals like basic gates, combinational and sequential logics in Digital System Design and Linear IC Applications**.**

(3) - Objectives and Outcomes:

The objectives of the course are to:

1. Give exposure to different steps involved in the fabrication of ICs.
2. Explain electrical properties of MOS and Bi-CMOS devices to analyze the behavior of Inverters designed with various loads.
3. Give exposure to the design rules to be followed to draw the layout of any logic circuit.
4. Provide design concepts to design building blocks of data path of any system using gates.
5. Understand basic programmable logic devices and testing of CMOS circuits.

Course Outcomes:

Course Code.CO	**Course Outcomes (CO's)**	**Blooms**
At the end of the course student will be able to		
C323.1	**Explain** fundamentals of IC technology and testing of CMOS circuits.	**BL2**

C323.2	**Choose** an appropriate inverter using electrical properties of MOS circuits.	**BL1**
C323.3	**Develop** layout of any logic circuit using concepts of stick diagrams and	**BL3**
C323.4	**Analyze** characteristics of different logic gates.	**BL4**
C323.5	**Design** memories and building blocks of data path of sub system.	**BL6**
C323.6	**Design** logic circuits using PLA's, PAL's, FPGA's and CPLD's.	**BL6**

(4)-Syllabus – R20 UGC Autonomous

UNIT – I
Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS and BiCMOS.
Basic Electrical Properties: Basic Electrical Properties of MOS and BiCMOS Circuits: I_{ds}-V_{ds} relationships, MOS transistor threshold Voltage, g_m, g_{ds}, Figure of merit; Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

UNIT - II
VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

UNIT – III
Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitance, Fan – in, Fan – out.

UNIT - IV
Data Path Subsystems: Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, Counters.
Array Subsystems: SRAM, DRAM, ROM, Serial Access Memories.

UNIT - V
Programmable Logic Devices: Design Approach – PLA, PAL, Standard Cells, FPGA's and CPLD's.
CMOS Testing: CMOS Testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

SYLLABUS - GATE

UNIT I

Device technology: integrated circuits fabrication process, oxidation, diffusion, ion implantation, photolithography, n-tub, p-tub and twin-tub CMOS process.

UNIT II

Not applicable

UNIT III
Not applicable

UNIT IV
Not applicable

UNIT V
Not applicable

SYLLABUS - IES

UNIT I
Basics of ICs - bipolar, MOS and CMOS types.

UNIT II
Not Applicable

UNIT III
Not Applicable

UNIT IV
NMOS, PMOS and CMOS gates.

UNIT V
Not Applicable

(5) - List of Expert Details(Local/National/International with Contact details/Profile link/Blogs/their research contribution towards the subject)

The Expert Details which have been mentioned below are only a few of the eminent ones known Internationally, Nationally and Locally. There are a few others known as well.

INTERNATIONAL

1. Mr.AnanthaP. Chandrakasan

   Professor of Electrical Engineering and Computer Science

   Massachusetts Institute of Technology

   e-mail: anantha@mtl.mit.edu

2. Dr. Hanho Lee

Professor School of Information and Communication Engineering

Inha University, Korea.

e-mail: hhlee@inha.ac.kr

NATIONAL

1. Dr. Cyril Prasanna Raj P. – Professor & Dean (R&D),

   M.S. Engineering College, Bangalore.

   e-mail: cyril@msec.ac.in

2. Dr. Navakanta Bhat

   Professor of Electrical Communication Engineering, IISC, Bangalore.

   e-mail: navakant@ece.iisc.ernet.in

REGIONAL

1. Dr. J. V. R. Ravindra, Professor Dept. of ECE,

   Vardhaman College of Engineering, Hyderabad.

   e-mail: jvr.ravindra@vardhaman.org

(6)- Journals with min 5 ref paper for literature study

INTERNATIONAL

1. ACM Transactions on Design Automation of Electronic Systems
2. IBM Journal of Research and Development
3. IEEE Transactions on CAD of Integrated Circuits and Systems
4. IEEE Transactions on Circuits and Systems Part I
5. IEEE Transactions on Circuits and Systems Part II
6. IEEE Transactions on Nanotechnology

   i) A novel multibridge-channel MOSFET (MBCFET): fabrication technologies and characteristics: https://ieeexplore.ieee.org/document/1264877

   ii) A comparative study on adders: https://ieeexplore.ieee.org/document/8300155

7. IEEE Transactions on VLSI Systems

iii) Design and analysis of low power SRAM cells:
https://ieeexplore.ieee.org/document/8244888

iv)Semiconductor for 5G: https://ieeexplore.ieee.org/document/8804702

v) Challenges and opportunities in nano-scale VLSI design :

https://ieeexplore.ieee.org/document/1500005

8. Integration, The VLSI Journal (Elsevier)
9. International Journal of Electronics (Taylor & Francis Group)
10. International Journal of Modeling and Simulation (ACTA Press)

vi) Design Of A Cmos Carry Look-Ahead Adder For Self-Timed Circuits:

https://www.tandfonline.com/doi/abs/10.1080/02286203.1997.11760338

11. IEEE Transactions on Circuits and systems
12. IEEE Transactions on Electronic Devices.
13. The Journal of VLSI Signal Processing (Kluwer)

NATIONAL

1. Journal of the Institute of Engineers
2. Journal of the Indian Institute of Science

i) VLSI-SoC: Research Trends in VLSI and Systems on Chip :
https://link.springer.com/book/10.1007/978-0-387-74909-9

3. IETE Journal of Education
4. IETE Journal of Research

ii) MOS and Bipolar Memory Circuit Techniques :

https://www.tandfonline.com/doi/abs/10.1080/03772063.1990.11436887

iii) A Low-power and High-performance Radix-4 Multiplier Design Using a Modified Pass-transistor Logic Technique : https://www.tandfonline.com/doi/abs/10.4103/0377-2063.81744

5. IETE Technical Review

(7)- Subject -Lesson plan

S.NO	Topic (JNTU syllabus)	Sub-Topic	cumulative Lectures Required	Suggested Books	Remarks

		UNIT - I	**08**		
1	Introduction to IC Technology	Classification and Applications of ICs and MOSFETS	L1, L2	**T1, R4**	
2	MOS, PMOS, NMOS, CMOS & BiCMOS	Fabrication of PMOS, NMOS, CMOS & BiCMOS	L3, L4	**T1, R4**	
3	Basic Electrical Properties of MOS and Bi CMOS Circuits	Operation of NMOS and PMOS	L5	**T1, R3**	
4	Ids-Vds relationships	Non saturated and saturated regions	L6,L7,	**T1, R3**	
5	MOS transistor parameters	MOS transistor threshold Voltage gm, gds, figure of merit ω_o	L8,L9	**T1, R3**	
6	Pass transistor, NMOS Inverter	Pass transistor, NMOS Inverter	L10	**T1, R3**	
7	Various pull-ups	NMOS and PMOS pull-ups	L11		
8	CMOS Inverter analysis and design	I-V characteristics of CMOS Inverter	L12	**T1, R3**	
7	Bi-CMOS Inverters	Various Bi-CMOS Inverters	L13, L14	**T1, R3**	Unit I completes on L14
		UNIT – II			
8	VLSI Design Flow	VLSI Design Flow	L15	**T1, R3**	
9	MOS Layers	N-Diffusion, P-Diffusion, Metal, Polysilicon, Silicon dioxide	L16, L17	**T1, R3**	
10	Stick Diagrams	Invereter, and logic gates Stick Diagrams	L18,L19	**T1, R3**	

11	Design Rules and Layout	Transistor Design Rules and Layout	L20	**T1, R3**	
12	Layout Diagrams for NMOS and CMOS Inverters and Gates	NMOS and CMOS Inverters and Gates for Layout Diagrams	L21	**T1, R2**	
13	Scaling of MOS circuits, Limitations of Scaling.	Scaling factors for device parameters	L22	**T1, R2**	Unit II completes on L22
		UNIT-III			
14	Logic Gates and Other complex gates	AND, OR, NAND, NOR and XOR logic Gates	L23	**T1, R2**	
15	Switch logic, Alternative gate circuits	Switch logic using Pass transistor, Domino logic, Pseudo NMOS, Dynamic logics.	L24, L25	**T1, R2**	
16	Time Delays, Driving large Capacitive Loads	Estimation of CMOS Invereter delay, Driving large Capacitive Loads.	L26	**T1, R2**	
17	Wiring Capacitances	Inter layer and Peripheral Capacitances.	L27	**T1, R2**	
18	Fan-in and fan-out, Choice of layers	Effects of Fan-in and fan-out, Choice of layers	L28	**T1, R2**	Unit III completes on L28
		UNIT – IV			
19	Subsystem Design	Datapath, Memory, Control and I/O cells	L29, L30	**T1, R2**	
20	Shifters, Adders	Barrel Shifter, Ripple carry adder	L31, L32	**T1, R2**	
21	ALU's, Multipliers	Array and Carry save Multipliers	L33	**T1, R2**	
22	Parity generators,	Parity generators,	L34	**T1, R2**	

	Comparators	Comparators			
23	Zero/One Detectors, Counters	Asynchronous and Synchronous Counters, Zero/One Detectors,	L35	**T1, R2**	
24	SRAM, DRAM, ROM	SRAM Array, Synchronous DRAM, EEROM	L36, L37	**T2, R2**	
25	Serial Access Memories	Serial Access Memories	L38, L39	**T2, R2,**	Unit IV completes on L39
		UNIT – V			
27	PLA's	Architecture of PLA's	L40, L41	**T2, R2**	
28	FPGA's, CPLD's	Architectures FPGA's, CPLD's	L42	**T2, R2**	
29	Standard cells	Types of ASIC's, MPGA's,	L43, L44	**T2, R2**	
30	Programmable Array Logic	Architecture of PAL's	L45		
31	Programmable Array Logic	Architecture of PAL's	L46, L47	**T2, R2**	
32	Design Approach, Parameters influencing low power design	Design Approach, Parameters influencing low power design	L48	**T2, R2**	
33	Design Approach, Parameters influencing low power design	Design Approach, Parameters influencing low power design	L49	**T2, R3**	
34	CMOS Testing, Need for testing	Functionality and Manufacturing test	L50	**T2, R1**	
35	Test Principles	Fault models, Fault coverage and Simulation	L51	**T2, R1**	
36	Design Strategies for test	DFT, Scan path	L52, L53	**T2, R1**	

37	System-level Test Techniques	TAP controller, BIST	L56, L57	**T2, R1**	
38	Chip level Test Techniques	Boundary Scan Chek, JTAG,	L54, L55	**T2, R1**	Unit IV completes on L57

(8) - Suggested Books (prescribed and References)

Text Books:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition
2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. CMOS logic circuit Design - John. P. Uyemura, Springer, 2007.
3. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.
4. VLSI Design- K. Lal Kishore, V. S. V. Prabhakar, I.K International, 2009.

(9) – Websites for self learning Resources like www.geeksforgeeks.org, www.schools.com, Coursera,edx,Udemy, Khan Academy, NPTEL etc along Registration Procedures

1. https://en.wikipedia.org/wiki/Very_Large_Scale_Integration
2. https://prezi.com/t6wpjvobwitw/very-large-scale-integration/
3. https://www.javatpoint.com/ic-fabrication-process
4. https://www.slideshare.net/varunkumar475/layout-stick-diagram-design-rules-60758496
5. https://www.oreilly.com/library/view/introduction-to-digital/9780470900550/chap5-sec003.html
6. https://in.coursera.org/learn/vlsi-cad-layout
7. https://in.coursera.org/learn/fpga-hardware-description-languages
8. https://nptel.ac.in/courses/106103016
9. https://www.udemy.com/course/cmos-digital-vlsi-for-beginners/
10. https://www.researchgate.net/publication/335503256_Performance_Improvement_in_VLSI_Adders

(10) – Question Bank – JNTUH

1. With neat sketches explain BICMOS fabrication process in an N well.

2. (a) With neat sketches, explain the transfer characteristic of a CMOS inverter.
   (b) Derive an equation for Ids of an n-channel enhancement MOSFET operating in saturation region.

3. Design a stick diagram and layout for the NMOS logic shown below
$Y = (A + B)C$.

4. (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
(b) In gate logic, compare the geometry aspects between two -input NMOS NAND and CMOS NAND gates.

5. (a) Draw the top level schematic and a floor plan for 16 × 16 Booth recoded multiplier and explain its operation.
(b) Explain the tradeoffs between open, closed, and twisted bit lines in a dynamic RAM array.

6. (a) Draw and explain the Antifuse Structure for programming the PAL device.
(b) Explain how the I/O pad is programmed in FPGA.

7. (a) Write a architecture for a 4- bit Counter in both behavioral and structural styles.
(b) Explain with example how mixed mode simulator is more for CMOS circuits testing.

8. (a) What are the reasons of malfunctioning of chip? What are the different levels of testing?
(b) Explain how a parallel scan is used for data path test.
(c) What is mean by level sensitive of logic system?

9. Write in detail about integrated passive components.

10. (a) Explain various regions of CMOS inverter transfer characteristics.
(b) For a CMOS inverter, calculate the shift in the transfer characteristic curve when $\beta n/\beta p$ ratio is varied from 1/1 to 10/1.

11. (a) Write the scaling factors for different types of device parameters.
(b) Discuss the limits due to sub threshold currents.

12. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.

13. (a) Draw the schematic for tiny XOR gate and explain its operation.
(b) Draw the circuit diagram for 4-by-4 barrel shifter using complementary transmission gates and explain its shifting operation.

14. (a) Draw and explain the Antifuse Structure for programming the PAL device.
(b) Explain how the I/O pad is programmed in FPGA.

15. (a) What type of defects are tested in manufacturing testing methods?
(b) What is the Design for Autonomous Test and what is the basic device used in this?
(c) What type of tests are used to check the noise margin for CMOS gates?

16. With neat sketches necessary, explain the oxidation process in the IC fabrication process.

17. (a) Draw an nMOS transistor model indicating all the components.
    (b) Explain latch up problem in CMOS circuits.

18. (a) Discuss in detail the NMOS design style.
    (b) Discuss CMOS design style. Compare with NMOS design style.

19. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.

20. (a) Explain how a Booth recoded multiplier reduces the number of adders.
    (b) Draw circuit diagram of a one transistor with transistor capacitor dynamic RAM and also draw its layout.

21. (a) Draw the typical standard-cell structure showing regular-power cell and explain it.
    (b) Draw and explain the pseudo-nMOS.PLA schematic for full adder and what are the advantages and disadvantages of it.

22. (a) Explain how function of system can be tested.
    (b) Explain any one of the method of testing bridge faults.
    (c) What type of faults can be reduced by improving layout design?

23. With neat sketches, explain in detail, all the steps involved in electron lithography process.

24. (a) Derive an equation for rds of an n channel enhancement MOSFET in linear region.
    (b) Plot the transfer characteristic of an nMOS inverter as a function of Vds.

25. (a) Discuss in detial the NMOS design style.
    (b) Discuss CMOS design style. Compare with NMOS design style.

26. (a) Explain the requirement and operation of pass transistors and transmission gates.
    (b) Compare pseudo-n MOS logic and clocked CMOS logic.

27. (a) How can the components of CMOS system design be categorized into the groups.
    (b) Why is the static 6 transistor cell used for average CMOS system design?
    (c) Compare the performance of CMOS Off chip and On chip memory designs.

29. (a) Draw a self timed dynamic PLA and what are the advantages of it compared to footed dynamic PLA.
    (b) Explain the tradeoffs between using a transmission gate or a tristate buffer to implement an FPGA routing block.

30. (a) Explain the gate level and function level of testing.
    (b) A sequential circuit with ‘n’ inputs and ‘m’ storage devices. To test this circuit how many

test vectors are required?
(c) What is sequential fault grading? Explain how it is analyzed.

31. With neat sketches explain the Ion -lithography process.
32. (a) Explain different forms of pull ups used as load, in CMOS and in enhancement & depletion modes of NMOS.
(b) Determine the pull up to pull down ratio of an nMOS inverter driven by another nMOS transistor.

33. Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions & layers.

34. Describe the following briefly
(a) Cascaded inverters as drivers.
(b) Super buffers.
(c) BiCMOS drivers.

35. Explain briefly the CMOS system design based on the data path operators, memory elements, control structures and I/O cells with suitable examples.

36. (a) Draw and explain the FPGA chip architecture.
(b) Draw and explain the AND/NOR representation of PLA.

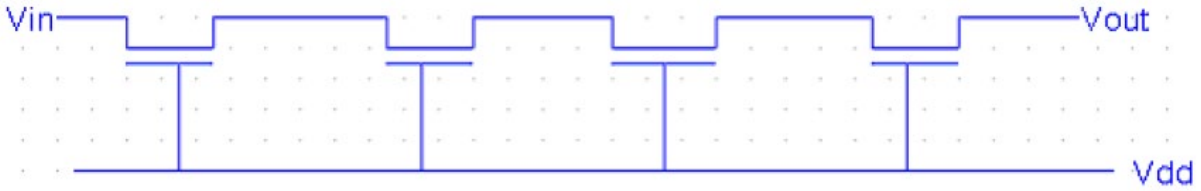
37. (a) Explain the gate level and function level of testing.
(b) A sequential circuit with in? inputs and 'm' storage devices. To test this circuit how many test vectors are required.
(c) What is sequential fault grading? Explain how it is analyzed.

38. Write in detail about integrated passive components.

39. (a) Explain the operation of BiCMOS inverter? Clearly specify its characteristics.
(b) Explain how the BiCMOS inverter performance can be improved.

40. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
(b) What are the effects of scaling on Vt?
(c) What are design rules? Why is metal- metal spacing larger than poly – poly spacing.

41. (a) Determine an equation for the propagation delay from input to output of the pass transistor chain shown in figure 4a with the help of its equivalent circuit.



(b) What are super Buffers?

42. (a) Explain how a Booth recoded multiplier reduces the number of adders.
(b) Draw circuit diagram of a one transistor with transistor capacitor dynamic RAM and also draw its layout.

43. (a) Draw the typical architecture of PAL and explain the operation of it.
(b) What is CPLD? Draw its basic structure and give its applications.

44. (a) What is ATPG? Explain a method of generation of test vector.
(b) Explain the terms controllability, observability and fault coverage.

45. Explain the MOS Transistor operation with the help of neat sketches in the following modes
(a) Enhancement mode
(b) Depletion mode

46. (a) Draw an nMOS transistor model indicating all the components.
(b) Explain latch up problem in CMOS circuits.

47. (a) What is Moore's law? Explain its relevance with respect to evolution of technology.
(b) What are different VLSI technologies available compare their speed/power performance.
(c) Why is VLSI design process presented in NMOS only?
(d) Discuss the micro electronics evolution.

48. (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
(b) In gate logic, compare the geometry aspects between two -input NMOS NAND and CMOS NAND gates.

49. (a) Design a magnitude comparator based on the data path operators.
(b) Draw the Schematic and mask layout of array adder used in Booth Multiplier and explain the principle of multiplication in Booth Multiplier.

50. (a) What are the characteristics of 22V10 PAL CMOS device and draw its I/O structure.
(b) Explain any one chip architecture that used the antifuse and give its advantages.

51. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
(b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register.

52. (a) With neat sketches explain the NMOS fabrication procedure.
(b) Draw the cross sectional view of CMOS P - Well inverter.

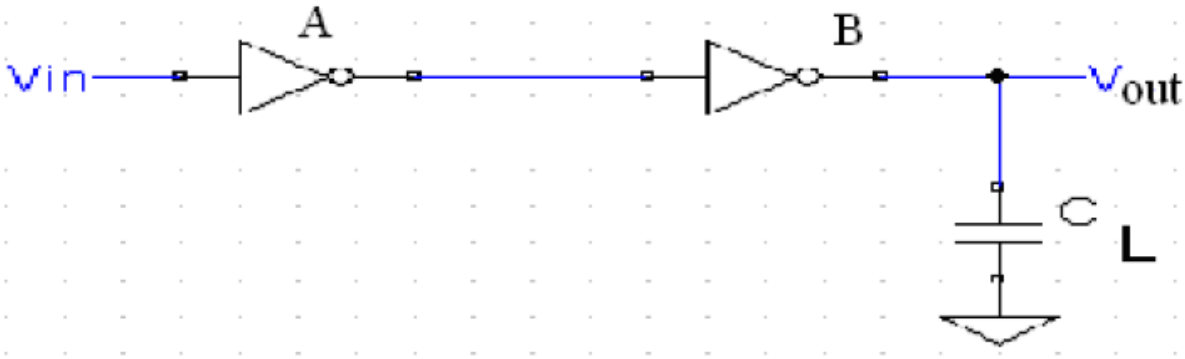
53. (a) Derive an equation for Transconductance of an n channel enhancement MOSFET operating in active region.
(b) A PMOS transistor is operated in triode region with the following parameters.

VGS=- 4.5V, Vtp= -1V; VDS=-2.2 V, (W/L) =95, μnCox =95μA/V 2. Find its drain current and drain source resistance.

54. (a) Discuss design rule for wires (orbit 2μm CMOS).
    (b) Discuss the transistor related design rule (orbit 2μm CMOS).

55. Two NMOS inverters are cascaded to drive a capacity load CL= 14Cg as shown in figure. Calculate the pair delay Vin to Vout in terms of τ for the given data.

    Inverter-A.
    Lpu=12λ, Wpu=4λ, Lpd=1λ, Wpd=8λ
    Inverter-B
    Lpu=4λ, Wpu=4λ, Lpd=2λ, Wpd=8λ



56. (a) Design a magnitude comparator based on the data path operators.
    (b) Draw the Schematic and mask layout of array adder used in Booth Multiplier and explain the principle of multiplication in Booth Multiplier.

57. Write briefly about:
    (a) Channeled gate arrays
    (b) Channel less gate arrays with neat sketches.

58. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
    (b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register.

59. (a) What is the principle of FPGAs? Explain about the architectures of FPGAs.
    (b) What are the applications of FPGAs? Explain.

60. Draw the circuit for NMOS Inverter and explain its operation.

61. (a) Explain the processing steps in fabrication of nmos technology with neat sketches.
    (b) Explain any one method of encapsulation of IC.

62. Write notes on any TWO

(a) DGT
(b) BIST
(c) Boundary scan Testing.

63. Give the topology for four bit carry select module and explain its operation in detail.

64. (a) Design a complimentary static CMOS XOR gate. Explain the steps involved and draw the logic circuit.
(b) What are the issues involved in driving large capacitor loads in VLSI circuit designs? Explain.

65. (a) Explain about the effect of scaling on MOSFET parameters.
i. Gate Area
ii. Gate capacitance
iii. Channel Resistance
iv. Transistor Delay
(b) Explain about Design Rules for contact cuts.

66. (a) Draw the circuit and layout schematic for 2-input NOR gate giving explanation.
(b) What are the various limitations of scaling?

67. Draw the circuit for CMOS inverter and explain the transfer characteristic using necessary equations, and the different regions in the characteristic.

68. (a) Give a schematic for memory self-test and explain the same.
(b) What are the advantages of implementing BIST? Explain.

69. What are the circuit design considerations in the case of static adder circuits?

70. (a) With the help of sketches explain the principles of different types of diffusion Processes.
(b) Explain about Fick's laws of diffusion.

71. (a) Explain the structure and principle of PLA.
(b) Draw the schematic and explain how Full Adder can be implemented using PLA's.

72. (a) Explain the concept of sheet resistance and sheet capacitance. Give examples.
(b) What are the design issues involved in long interconnect wires? Explain.

73. (a) Explain the processing steps in fabrication of PMOS technology with neat sketches.
(b) What are the additional two layers in BICMOS technology compared to others?

74. (a) Explain about stick diagram.
(b) Explain about scaling.

75. (a) Draw the circuit of CMOS Inverter and explain its operation.

(b) What are the various pull up transistor used for inverters?

76. (a) What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.
(b) Derive the expression for τ_{SD} in the case of a MOSFET.

77. (a) With the help of a schematic explain about Memory-self Test.
(b) What are the issues to be considered while implementing BIST? Explain.

78. Draw the schematic for Wallace Tree for four bit Multiplier and explain its operation.

79. (a) Draw the structure of programmable Array logic(PAL) and explain its principle of operation.
(b) Explain about different methods of implementation approaches in VLSI Design.

80. Explain the principle and working of CPLDs and give their applications.

81. (a) With the help of flow chart explain the method of Testing at various stages in VLSI Design cycle.
(b) Why testing is needed in VLSI design? Explain the principle of testing.

82. Draw the circuits for n-MOS, p-MOS and C-MOS Inverter and explain about their operation and compare them.

83. (a) Explain about bit sliced Data path organization. What is the significance of Data paths in digital processors?
(b) Give the Truth Table for full adder and explain its Boolean expression.

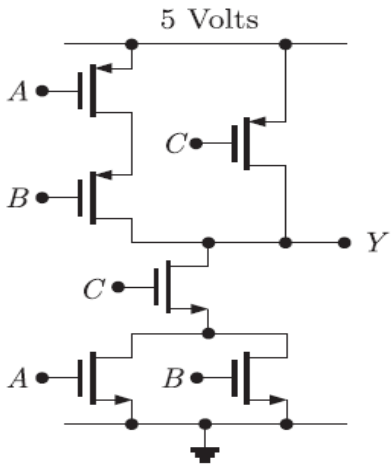
84. (a) What are the different types of oxidation processes? Explain.
(b) With the help of neat sketches, explain the steps involved in photolithography and pattern transfer.

85. Explain about Static Logic, Dynamic Logic and Domino Logic and compare them in all respects.

86. (a) Why scaling is required?
(b) How does Depletion Regions around Source and Drain are affected due to scaling down of device dimensions? Explain.

(10.2) *QUESTION BANK – GATE*

1. In the circuit shown GATE 2012

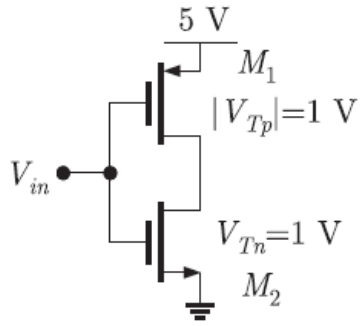


(A) $Y = \overline{A}\,\overline{B} + \overline{C}$ (B) $Y = (A + B)\,C$

(C) $Y = (\overline{A} + \overline{B})\,\overline{C}$ (D) $Y = AB + C$

2. In the CMOS circuit shown, electron and hole mobilities are equal, and $M1$ and $M2$ are equally sized. The device $M1$ is in the linear region if

GATE 2012

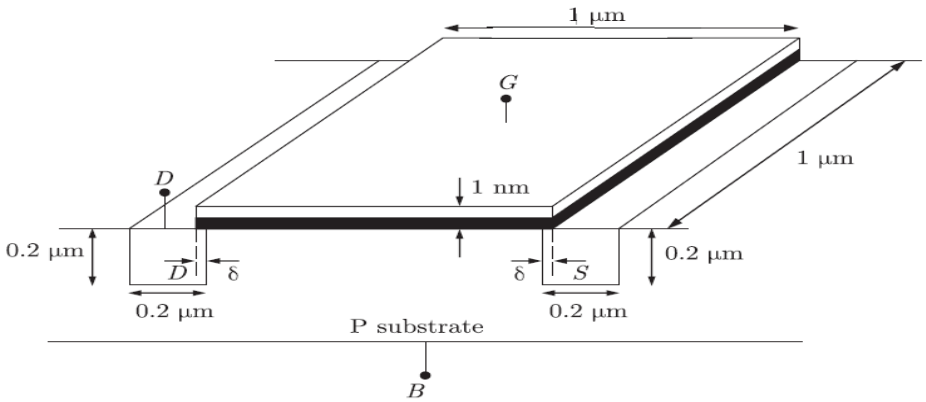


(A) Vin < 1.875 V (B) 1.875 V <Vin < 3.125 V

(C) Vin > 3.125 V (D) 0 <Vin < 5 V

Common Data for Question 3 and 4 : GATE 2012

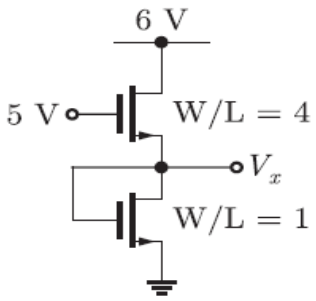
In the three dimensional view of a silicon n-channel MOS transistor shown below, δ = 20 nm. The transistor is of width 1 μm. The depletion width formed at every p-n junction is 10 nm. The relative permittivity of Si and SiO2, respectively, are 11.7 and 3.9, and ε_O= 8.9 X 10 F/m



3. The gate source overlap capacitance is approximately
(A) 0.7 fF (B) 0.7 pF
(C) 0.35 fF (D) 0.24 Pf

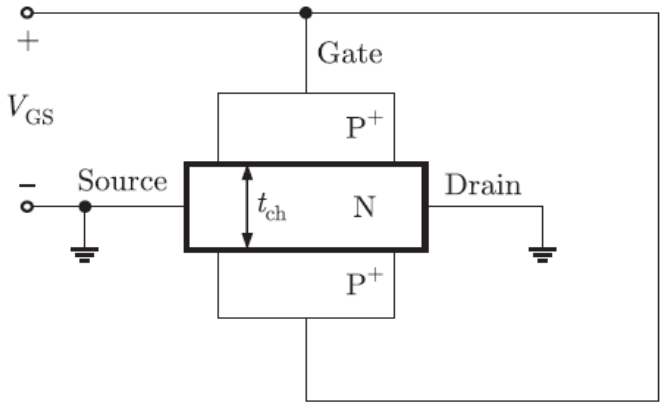
4. The source-body junction capacitance is approximately
(A) 2 fF (B) 7 fF
(C) 2 pF (D) 7 pF

5. In the circuit shown below, for the MOS transistors, μ $nCox$ 100 A/V^2 and the threshold voltage VT = 1V. The voltage Vx at the source of the upper transistor is
GATE 2011



(A) 1 V (B) 2 V
(C) 3 V (D) 3.67 V

Common Data Questions: 6 & 7 GATE 2011
The channel resistance of an N-channel JFET shown in the figure below is 600 Ω when the full channel thickness (*tch*) of 10μm is available for conduction. The built in voltage of the gate *P*+ *N* junction (*Vbi*) is −1V. When the gate to source voltage (*VGS*) is 0 V, the channel is depleted by 1 μm on each side due to the built in voltage and hence the thickness available for conduction is only 8 μm



6. The channel resistance when $VGS = -3$ V is
(A) 360 Ω (B) 917 Ω
(C) 1000 Ω (D) 3000 Ω

7. The channel resistance when $VGS = 0$ V is
(A) 480 Ω (B) 600 Ω
(C) 750 Ω (D) 1000 Ω

8. At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon *n*-channel MOSFET is
GATE 2010
(A) 450 cm^2 /V-s (B) 1350 cm^2 /V-s
(C) 1800 cm^2 /V-s (D) 3600 cm^2 /V-s

9. Thin gate oxide in a CMOS process in preferably grown using
GATE 2010
(A) wet oxidation (B) dry oxidation
(C) epitaxial oxidation (D) ion implantation

(10.3) QUESTION BANK – IES

1. A gate to drain-connected enhancement mode MOSFET is an example of IES 2012
(a) an active load (b) a switching device
(c) a three-terminal device (d) a three-terminal device

2. Body effect in MOSFETs results in IES 2012
(a) increase in the value of transconductance
(b) change in the value of threshold voltage
(c) decrease in the value of transconductance

(d) increase in the value of output resistance

3. Assertion !A) : Si mainly used for making lCs and not Ge. IES 2011

Reason(R) : In Si, Si02 layer which acts as an insulator can be formed for isolation purposes. Corresponding oxide layer cannot be formed in Ge.

(11) - Two case study presentationswith Project / Product/ Model /prototypes/ Industrial applications:

1. Design of a Multiplexer In Multiple Logic Styles for Low Power VLSI

The Low power and low energy has become an important issue in today's consumer electronics. Any combinational circuit can be represented as a multiple inputs with single output. Multiplexers are used to design any digital combinational logic circuit. Hence it is required to design a multiplexer with low power consumption and high speed. The main objective of this paper is to design the multiplexer using complementary metal oxide semiconductor (CMOS) logic and pass-transistor logic styles. The power consumption, delay, area, transistor count of various logic styles are compared. This paper shows that static NMOS logic multiplexer is an optimum device level design which has characteristics of high speed with minimum power compared with other realizations. These different logic styles are compared by performing detailed transistor level simulations using CAD tools of DSCH3 and Micro wind 3.1 in submicron regime.

2. Performance Improvement in VLSI Adders

In modern electronics, an adder is a digital circuit that computes the sum of numbers. In many mainframe computers and other processors, adders are used both in the arithmetic logic unit (ALU), and also in various other parts of the computer; they are used to compute addresses, table indices, and various other operations. In VLSI technology, adders have gained a lot of importance. The data processed by numerous digital systems may have delays. Area efficient and power efficient high speed data path logic system designs are one of the important domains of research in VLSI system design. The demand and reputation of portable electronics is motivating the designers to achieve smaller silicon area, longer battery life, higher speeds, and more reliability. Power is one of the important resources a designer tries to save while designing a system. Full adders are fundamental units in various complex circuits, especially in circuits for performing arithmetic operations such as comparators, compressors, parity checkers and so on. Full adders are mainly present in the critical paths of complex arithmetic circuits for multiplication and division. In digital adders, the time required to propagate a carry through the adder limits the speed of addition. The main objective is to minimize the area, delay, power and memory of various types of adders in VLSI System design.

(12) - Assignment Question sets:

<u>Unit – I</u>

SET 1:

1. With neat sketches explain the electron lithography process.

2. Derive the relationship between drain current Id versus drain to source voltage Vds in active region and saturation region.

3. What are different forms of Pull – ups? Determine the Pull-up to Pull – down of an NMOS Inverter driven by another NMOS Transistor.

4. Explain the advantages of MOS technology over the bipolar technology and why MOS devices gained predominance over bipolar devices?

SET 2:

1. Explain the operation of BiCMOS inverter? Clearly specify its characteristics.

2. Explain the various steps in PMOS Fabrication.

3. Explain the process flow of CMOS Fabrication.

4. Compare NMOS & CMOS Technologies.

SET 3:

1. Describe the two commonly used methods for obtaining integrated capacitor.
2. With neat sketches, explain in detail, all the steps involved in electron lithography process.
3. What is Moore's law? Explain its relevance with respect to evolution of ICTechnology.
4. What is the size of silicon wafer used for manufacturing state-of-the art VLSIICs?

SET 4:

1. What is the minimum feature size of current commercial VLSI devices?
2. Explain the following:

(a) Thermal oxidation technique

(b) Kinetics of thermal oxidation.

3. With neat sketches explain how NPN transistor is fabricated in bipolar process.
4. With neat sketches explain how Diodes and Resistors are fabricated in NMOS Process.

Unit – II

SET 1:

1. Size the devices and draw the stick diagram of a CMOS, and NMOS inverter circuits.

2. Do the NMOS and CMOS implementations of the circuit for function whose logic is given by Also draw it's layout:

$$Y = (A+B).C$$

3. Derive the propagation delay of a depletion mode n-channel MOSFET.

4. Derive the pull-down ratio of a CMOS inverter.

SET 2:

1. Derive the pull-up to pull-down ratio of a CMOS inverter.
2. What is a stick diagram? Draw the stick diagram and layout for a CMOS Inverter.

3. What are the effects of scaling on Vt?

4. What are design rules? Why is metal- metal spacing larger than poly –poly spacing.

SET 3:

1. Draw the stick diagram and mask layout for a CMOS two input NOR gate andStick diagram of two input NAND gate.

2. Draw the stick diagram and a translated mask layout for nMOS inverter circuit.

3. Explain the following
(a) Double metal MOS process rules.
(b) Design rules for P- well CMOS process

4. Design a stick diagram for two input n-MOS NAND and NOR gates.

SET 4:

1. Design a stick diagram for the NMOS logic shown below $Y = (A + B + C)'$.

2. Design a stick diagram for n-MOS Ex-NOR gate.

3. Design a stick diagram for the PMOS logic shown below $Y = ((A + B).C)'$.

4. Design a layout diagram for the PMOS logic shown below $Y = (AB)' + (CD)'$.

Unit - III

SET 1:

1. Implement the logic diagram for the Boolean equation Y = (A+B).(C+D) after sizing the transistors. Do the NMOS and CMOS implementations.

2. Do the NMOS and CMOS implementations of the circuit for the function whose logic is given by Y = (A+B).C

3. Explain how the resistance of a non-rectangular region can be measured?

4. Calculate the rise time and fall time of the CMOS inverter (W/L)n= 6 and (W/L)p=8,K′n =150μ A/V 2, Vtn=0.7V, K′p= 62 μ A/V 2, Vtp=-0.85V, VDD =3.3V. Total out-put capacitance =150 fF.

SET 2:

1. Explain the concept of sheet resistance and apply it to compute the ON resistance (VDD to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is Rsn = 10^4 per square.

2. Calculate the gate capacitance value of 5μm technology minimum size transistor with gate to channel capacitance value is 4×10^{-4}pF/μm2.

3. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.

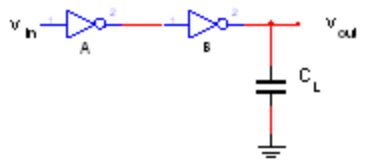
4. Define and explain the following:
i. Sheet resistance concept applied to MOS transistors and inverters.
ii. Standard unit of capacitance.

SET 3:

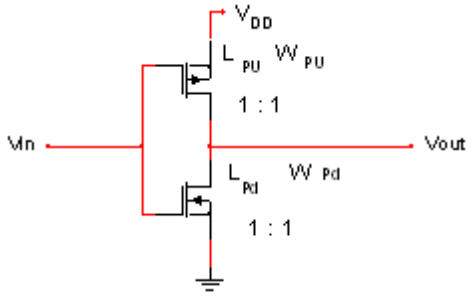
1. Explain the requirement and functioning of a delay unit.

2. Two nMOS inverters are cascaded to drive a capacitive load CL=14Cg as shown inFigure. Calculate the pairdelay Vin to Vout in terms of τ for the given data.

Inverter -A
LP.U= 12λ , WP.U = 4 λ , LP.d = 1 λ , WP.d = 1 λ
Inverter -B
LP.U= 4λ , WP.U = 4 λ , LP.d = 2 λ , WP.d = 8 λ



3. Calculate on resistance of the circuit shown in Figure 1 from VDD to GND. If n-Channel sheet resistance Rsn = 10 4 per square and p-channel sheet resistance Rsp = 2.5 × 104 per square.



4. Calculate the gate capacitance value of 2µm technology minimum size transistorwith gate to channel capacitancevalue is 8 × 10−4pF/µm2.

SET 4:

1. Explain clearly about different parasitic capacitances of an nMOS transistor.

2. Do the NMOS and CMOS implementations of the circuit for the function whose logic is given by Y = (A+B).C

3. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of aVLSI circuit.

4. Explain how the resistance of a non-rectangular region can be measured?

Unit - IV

SET 1:

1. Design a logic gate network for the full adder using two-level logic; using multi-level logic.

2. What is the false delay path in the carry-skip adder?

3. Design the logic for an ALU that can perform these functions: addition, subtraction, AND, OR, NOT.

4. Design components of a Booth multiplier.

SET 2:

1. Design the logic for one bit of the adder-subtractor.
2. Design a stick diagram for adder-subtractor.
3. Design and analyze an 8 x 8 Wallace tree multiplier.
4. Draw the block diagram for an eight-bit carry save adder.

SET 3:

1. Draw the complete block diagram for the 8 x 8 Wallace tree multiplier.
2. What is the minimum-delay encoding for a modulo-8 counter?

3. Explain the CMOS system design based on the data path operators with asuitable example.

4.Draw and explain the basic Memory- chip architecture.

SET 4:

1. Explain the CMOS system design based on the data path operators with asuitable example.

2. Draw and explain the basic Memory- chip architecture.

3. Compare the different types of CMOS subsystem Multipliers.

4. Design a schematic for an 8-word × 2-bit NAND ROM that serves a lookuptable to implement a full adder.

Unit –V

SET 1:

1. What are the advantages and disadvantages of ASIC design approach?
2. Give the block diagram of PLA device and explain about the PLA.
3. Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
4. Explain how ROM can be used as PLD.

SET 2:

1. Explain about the three different approaches for the formation of logic cell using FPGA implementation.
2. Explain the function of 4:1 Mux in PAL CMOS device with the help of I/O structure.
3. Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming.
4. Explain the methods of programming of PAL CMOS device.

SET 3:

1. Draw and explain the architecture of an FPGA.
1. Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
2. Explain any one chip architecture that used the antifuse and give its advantages.
3. Draw the typical standard-cell structure showing low-power cell and explain it.

SET 4:

1. Sketch a diagram for two input XOR using PLA and explain its operation with the help of truth table.
2. Using PLA Implement JK Flip flop circuit.
3. With neat sketches explain the architecture of PAL.
4. Explain about the different test techniques such as scan based, self test and IDDQ testing.

(13) - List of topics for students Seminars

1. Static Timing Analysis
2. Analog Memories
3. Nano-RAM
4. Organic LED
5. M-RAM(Magneto Resistance Random Access Memory)
6. Multi Threshold CMOS

7. Low Leak Transistor
8. MESFET
9. Single Electron Tunneling Technology
10. Extreme Ultra Violet Lithography
11. MEMS (Micro Electro Mechanical Systems)
12. Photonic Integration of Hybrid Silicon

(14) - STEP/Course material in softcopy

1. How do you prevent latch up problem?

Latch up problem can be reduced by reducing the gain of parasitic transistors and resistors. It can be prevented in 2 ways

•Latch up resistant CMOS program •Layout technique

The various lay out techniques are

Internal latch up prevention technique

I/O latch up prevention technique.

2. List the basic process for IC fabrication

Silicon wafer Preparation _ Epitaxial Growth

Oxidation

Photolithography _ Diffusion

Ion Implantation _ Isolation technique _ Metallization

Assembly processing & Packaging

3. What are the various Silicon wafer Preparation?

Crystal growth & doping

Ingot trimming & grinding _ Ingot slicing

Wafer polishing & etching _ Wafer cleaning.

4. Different types of oxidation?

Dry & Wet Oxidation

5.What are the advantages of CMOS process?

Low power Dissipation High Packing density Bi directional capability Low Input Impedance Low delay Sensitivity to load.

6.What is pull down device?

A device connected so as to pull the output voltage to the lower supply voltage usualy 0V is called pull down device.

7.What is pull up device?

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

8.. Why NMOS technology is preferred more than PMOS technology?

N- channel transistors has greater switching speed when compared tp PMOS transistors.

9. What are the different operating regions foe an MOS transistor?

_ Cutoff region

_ Non- Saturated Region _ Saturated Region

10.What is Channel-length modulation?

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied VDS, increasing VDS causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

11. What is Latch – up?

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

UNIT-2

1.What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

2. What are the uses of Stick diagram?

It can be drawn much easier and faster than a complex layout.

These are especially important tools for layout built from large cells.

3. Give the various color coding used in stick diagram?

_ Green –n-diffusion _ Red- polysilicon

_ Blue –metal

_ Yellow- implant

_ Black-contact areas.

4. Define Threshold voltage in CMOS?

The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

5. What is Body effect?

The threshold voltage VT is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

6**. What are the various CMOS technologies?**

Various cmos technologies are,

I) n- well process or n -tub process

ii)p well process or p-tub process

iii)Twin tub process

iv)Silicon on Insulator (SOI) process

7.What is channel-stop implantation?

In n -well fabrication, n-well is protected with resist material. Because it should not be affected by boron implantation. Then boron is implanted except n-well. It is done using photo resist mask. This type of implantation is known as channel-stop implantation.

8. What is LOCOS?

LOCOS mean Local Oxidation of Silicon. This is one type of oxide construction.

9. What is LDD?

LDD means Lightly Doped Drain structures. It is used for implantation of n-in n-well process. **10. What is twin tub process? Why it is so called?**

Twin tub process is one of cmos technology. There are two wells available in this process. The other name of well is tub. so because of these two tubs, this process is known as twin tub process.

11. What are the special features of twin tub process?

In twin tub process, threshold voltages, body effect of n and p devices are independently optimized.

12. What are the advantages of twin tub process?

Advantages of twin tub process are

1)Separate optimized wells are available.

2)Balanced performance is obtained for n and p transistors.

16.What is meant by interconnect? What are the types of interconnect?

Interconnect means connection between various components in an IC Types of Interconnect

Metal Interconnect

Polysilicon Inter connect.

Local Inter Connect.

17.What are the two types of Layout design rules?

Lambda (λ) design rules and micron rules are major types of layout design rules.

18. What is pull down device?

A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

19. What is pull up device?

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21. What are the different operating regions for an MOS transistor?

_ Cutoff region

_ Non- Saturated Region _ Saturated Region

22. What are the different MOS layers?

N- Diffusion

P- Diffusion

SIO2

UNIT 3

1. **Which MOS can pass logic1 and logic 0 strongly?**

p-mos can pass strong logic 1n-mos can pass strong logic 0.

2. What is meant by a transmission gate?

A transmission gate consists of an n-channel transistor and p-channel transistor with separate gates and common source and drain. Its symbol is

3. Write the design style classification?

The IC design style can be classified as

(1)Full custom Design ASICs

(2)Semi custom Design ASICs

(a)Standard Cell Design

(b)Gate Array Design

(i)Channeled Gate Array

(ii)Channel less Gate Array

(3)Programmable ASICs

(a)PLDs

(b)FPGA

4. What are the two types of ASICs ?

Types of ASICs are

Full custom ASICs

Semi custom ASICs

5. What are the types of programmable devices?

Types of programmable devices are

(1)Programmable Logic Structure

(2)Programmable Interconnect.

(3)Reprogrammable Gate Array.

6. What are the different types of programming structure available in PAL?

Programming Techniques of PAL are

(1)Fusible links programming

(2)UV-Erasable EPROM programming

(3)EEPROM programming

7. Why CMOS technology is most useful for analog functions?

The first reason is that CMOS is now by far the most widely available IC technology. Most CMOS Asics and CMOS standard products are now being manufactured than bipolar ICs. The second reason is that increased levels of integration require mixing analog and digital functions on the same IC: this has forced designers to find ways to use CMOS technology to implement analog functions.

UNIT-4

1. What are the features of standard celled ASICs?

All mask layers are customized- transistors and interconnect.

Custom blocks can be embedded.

Manufacturing lead time is about eight weeks.

2. What is the difference between channeled gate array and channel less gate array?

The key difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate –array devices. We can do this because we customize the contact defines the connections between metal1, the first layer of metal and the transistors.

3. What are the characteristics of FPGA?

None of the mask layers are customized

•A method for programming the basic logic cells and the interconnect.

•The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).

•A matrix of programmable interconnect surrounds the basic logic cells.

•Design turnaround is a few hours.

4. What is programmable logic array?

A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an output an output. This layout allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

6. What is mean by Programmable logic plane?

The Programmable logic plane is programmable read-only memory (PROM) array that allows the signals present on the devices pins (or the logical components of those signals) to be routed to an output logic macro cell.

7. Describe the steps in ASIC design flow?

•Design entry. Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry.

•Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a net list

– a description of the logic cells and their connections.

•System partitioning. Divide a large system into ASIC- sized pieces.

•Prelayout simulation. Check to see if the design functions correctly.

•Floor planning. Arrange the blocks of the net list on the chip.

•Placement. Decide the locations of cells in a block.

•Routing. Make the connections between cells and blocks.

•Extraction. Determine the resistance and capacitance of the interconnect.

•Post layout simulation. Check to see the design still works with the added loads of the inter connect.

8. Give the application of PLA

Design and testing of digital circuits

17. What is the full custom ASIC design?

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

9. What is the standard cell-based ASIC design?

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

10. Give the constituent of I/O cell in 22V10.

2V10 I/O cell consists of

1.a register

2.an output 4:1 mux

3.a tristate buffer

4.a 2:1 input mux

It has the following characteristics:

*12 inputs

*10 I/Os

*product time 9 10 12 14 16 14 12 10 8

*24 pins

11. What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

12. What are the different methods of programming of PALs?

The programming of PALs is done in three main ways: Fusible links

UV – erasable EPROM

EEPROM (E 2PROM) – Electrically Erasable Programmable ROM.

14. What are the different levels of design abstraction at physical design? Architectural or functional level

Register Transfer-level (RTL) Logic level

Circuit level

15.What are macros?

The logic cells in a gate-array library are often called macros.

16. What are Programmable Interconnects?

In a PAL, the device is programmed by changing the characteristics of the switching element. An alternative would be to program the routing.

17. What are the types of gate arrays in ASIC?

1) Channel gate arrays

2) Channel less gate arrays

3) Structured gate arrays

18. Mention the common techniques involved in ad hoc testing?

Partitioning large sequential circuits

Adding test points

Adding multiplexers

providing for easy state reset

19.What are the scan-based test techniques?

a) Level sensitive scan design

b) Serial scan

c) Partial serial scan

d) Parallel scan

20.What are the two tenets in LSSD?

a. The circuit is level-sensitive.

b. Each register may be converted to a serial shift register.

21. What are the self-test techniques?

a. Signature analysis and BILBO

b. Memory self-test

c. Iterative logic array testing

22. What is known as BILBO?

Signature analysis can be merged with the scan technique to create a structure known as BILBO- for Built In Logic Block Observation.

23. What is known as IDDQ testing?

A popular method of testing for bridging faults is called IDDQ or current supply monitoring. This relies on the fact that when a complementary CMOS.

Logic gate is not switching, it draws no DC current. When a bridging fault occurs, for some combination of input conditions a measurable DC IDD will flow.

24. What are the applications of chip level test techniques?

a. Regular logic arrays

b. Memories

c. Random logic

26. What is boundary scan?

The increasing complexity of boards and the movement to technologies like multichip modules and surface-mount technologies resulted in system designers agreeing on a unified scan-based methodology for testing chips at the board. This is called boundary scan.

27. What is the test access port?

The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in a boundary-scan architecture. The port has four or five single bit connections, as follows:

TCK (The Test Clock Input)

TMS (The Test Mode Select) TDI(The Test Data Input) TDO(The Test Data Output)

It also has an optional signal TRST*(The Test Reset Signal).

28. What are the contents of the test architecture?

The test architecture consists of:

The TAP interface pins A set of test-data registers An instruction register

A TAP controller

29. What is the TAP controller?

The TAP controller is a 16-state FSM that proceeds from state to state based on the TCK and TMS signals. It provides signals that control the test data registers, and the instruction register. These include serial-shift clocks and update clocks.

30. What is known as test data register?

The test-data registers are used to set the inputs of modules to be tested, and to collect the results of running tests.

31. What is known as boundary scan register?

The boundary scan register is a special case of a data register. It allows circuit-board interconnections to be tested, external components tested, and the state of chip digital I/Os to be sampled.

32. Mention the levels at which testing of a chip can be done?

a) At the wafer level

b) At the packaged-chip level

c) At the board level

d) At the system level

e) In the field

33. Expert Lectures with topics & Schedules (if any)

Stick diagrams and Layouts on the month of February.

Emerging Issues in VLSI Design on the month of March.

UNIT 5

1. What are the different types of CMOS testing

Functionality tests manufacturing tests

2. What is the aim of adhoc test techniques?

The adhoc test techniques are aimed at reducing the combinational explosion of testing.

3. Distinguish functionality test and manufacturing test

Functionality tests seek to verify that a chip as a whole is functionally equivalent to some specification, whereas manufacturing tests are used to verify that every gate operates as expected.

4. List any two faults that occur during manufacturing

1. Stuck at fault

(a)Stuck at 0 fault

(b)Stuck at 1 fault

2.SC & OC faults

(a)Short circuit model fault

(b)Open circuit model fault

5. What is the need for testing?

IC fabrication is very complex process. SO, there may be any imperfection occur in any one of the stage. This imperfection may affect the result. So testing is necessary to find out which IC is good and which IC is bad.

6. Write notes on functionality tests?

Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.

7. Write notes on manufacturing tests?

Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.

8.Mention the defects that occur in a chip?

a)layer-to-layer shorts

b) discontinuous wires

c)thin-oxide shorts to substrate or well

9.Give some circuit maladies to overcome the defects?

i. nodes shorted to power or ground

ii. nodes shorted to each other

iii. inputs floating/outputs disconnected

10.What are the tests for I/O integrity?

i.I/O level test

ii.Speed test

iii.IDD test

11. What is meant by fault models?

Fault model is a model for how faults occur and their impact on circuits.

12.Give some examples of fault models?

i.Stuck-At Faults

ii.Short-Circuit and Open-Circuit Faults

13.What is stuck – at fault?

With this model, a faulty gate input is modeled as a "stuck at zero" or "stuck at one". These faults most frequently occur due to thin-oxide shorts ormetal-to-metal shorts.

14. What is meant by observability?

The observability of a particular internal circuit node is the degree to which one can observe that node at the outputs of an integrated circuit.

15. What is meant by controllability?

The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

16. What is known as percentage-fault coverage?

The total number of nodes that, when set to 1 or 0, do result in the detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage.

17. What is fault grading?

Fault grading consists of two steps. First, the node to be faulted is selected. A simulation is run with no faults inserted, and the results of this simulation are saved. Each node or line to be faulted is set to 0 and then 1 and

the test vector set is applied. If and when a discrepancy is detected between the faulted circuit response and the good circuit response, the fault is said to be detected and the simulation is stopped.

18.Mention the ideas to increase the speed of fault simulation?

a. Parallel simulation

b. Concurrent simulation

19. What is fault sampling?

An approach to fault analysis is known as fault sampling. This is used in circuits where it is impossible to fault every node in the circuit. Nodes are randomly selected and faulted. The resulting fault detection rate may be statistically inferred from the number of faults that are detected in the fault set and the size of the set. The randomly selected faults are unbiased. It will determine whether the fault coverage exceeds a desired level.

20. What are the approaches in design for testability?

a.ad hoc testing

b.scan-based approaches

c.self-test and built-in testing

21.Mention the common techniques involved in ad hoc testing?

d.partitioning large sequential circuits

e.adding test points

f.adding multiplexers

g.providing for easy state reset

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(15) - Expert Lectures with topics & Schedules (if any)

S.NO	SUBJECT	TOPIC	YEAR	RESOURCE PERSON	DATE
1	VLSID – EL01	Layout and Stick Diagram	III-II	Others	Jan,2023
2	VLSID - EL02	Emerging Issues in VLSI Design	III-II	Others	March,2023

FPGA PROGRAMMING

Subject Code: EC622PE

Class: III-Year B.Tech ECE II-Semester

BY

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CMR ENGINEERING COLLEGE

S.NO **CONTENT**

(1) - Preamble/Introduction
(2) - Prerequisites
(3) - Objectives and Outcomes
(4) - Syllabus
1.JNTU/R20-CMREC
2.GATE
3.IES
(5) - List of Expert Details(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6) - Journals with min 5 ref paper for literature study
(7) - Subject -Lesson plan
(8) - Suggested Books (prescribed and References)
(9) - Websites for self learning Resources like *www.geeksforgeeks.org, www.schools.com, Coursera, edX, Udemy, Khan Academy*, NPTEL etc along Registration procedures*)*
(10) - Question Banks
1.JNTUH/Model papers
2.GATE
(11) - Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications.
(12) - Assignment Question/Innovative Assignments sets.
(13) -List of topics for students Seminars with Guidelines
(14) - STEP/Course material in softcopy

(15) - Expert Lectures with topics & Schedules

1. Preamble/Introduction:

This course deals with logical device design with programmable logic devices (PLDs). With ongoing advance in electronics, these devices have grown significantly in capability and complexity. The two most interesting types of PLDs: C(complex)PLD and FPGA (Field Programmable Gate Arrays) are the focus of the subject. Being programmable, have the important capability of being re-configurable. They can be reprogrammed to rapidly realize another function. This valuable capability can easily seduce the unwary designer into a design trap. Quickly produce an inferior design with the intent on reconfiguring to a better design later.

The applications of this course include Video imaging, Military technologies, including missile guidance systems, Automotive computing, Aerospace applications, Search engine algorithms, Networking and datacenter management, Signal processing, Medical devices etc.

2. Prerequisites:

This course recommends basic knowledge and practice on Digital System Design and Digital IC's.

3. Objectives:

1. Give exposure to different types of PLDs.
2. Explain the Universal Design Methodology for Programmable Devices.
3. Give exposure to the Data flow Description and Behavioral Description.
4. Give exposure to the Structural and Switch level Descriptions.
5. Understand Procedures, Tasks, Functions and Verification.

Outcomes:

Upon completion of the course, students will be able to:

1. Explain the Architecture of SPLD's, CPLD's and FPGA's.
2. Analyze the Universal Design Methodology for Programmable Devices.
3. Design Digital circuits using Data flow and Behavioral Descriptions.
4. Design Digital circuits using Structural and Switch level Descriptions.
5. Analyze mixed type descriptions, Procedures, Tasks and understand about formal verification.

4.

R20 CMREC

UNIT-I

Simple Programmable Logic Devices (SPLD's):

Programmable Read Only Memories (PROMs), Programmable Logic Arrays (PLAs), Programmable Array Logic (PALs), the Masked Gate Array ASIC.

Complex Programmable Logic Devices (CPLD's):

CPLD Architectures, Function Blocks, I/O Blocks, Clock Drivers, Interconnect CPLD Technology and Programmable Elements, Embedded Devices.

Field Programmable Gate Arrays (FPGA's):

FPGA Architectures, Configurable Logic Blocks, Configurable I/o Blocks, Embedded Devices, Programmable Inter Connect, Clock Circuitry, SRAM vs. Anti-fuse programming, FPGA Selection Criteria.

UNIT – II

Universal Design Methodology for Programmable Devices:

Introduction to UDM and UDM-PD, writing a Specification, Specification Review, Choosing Device and Tools, Design, Verification, Final Review, System Integration and Test. Hardware Descriptive Languages, Structure of VHDL & Verilog module, operator, Data types, Top-Down Design, Synchronous Design, Floating Nodes, Bus Contention, One-Hot state Encoding.

UNIT –III

Data flow Description and Behavioral Descriptions:

Introduction to styles types of hardware description –Behavioral, Structural, Dataflow and Mixed type and language descriptions.

Data flow Description: Structure of the dataflow description, Signal Declaration and Assignment Statements, Concurrent Signal assignments, Constant declaration and assignments, assigning a delay time to the signal, Data type-Vectors.

Behavioral Descriptions: Structure of the HDL Behavioral description, The VHDL/ Verilog HDL variable – assignment statement, sequential statement – IF, signal and variable assignment, CASE & LOOP statements.

UNIT –IV

Structural and Switch level Descriptions:

Structural Description: Organization of the structural description, binding, state machines, Generate (HDL), Generic (VHDL), and parameter (Verilog).

Switch level Description: Useful definitions, Single NMOS & PMOS switches-verilog & VHDL description of NMOS & PMOS Switches, serial and parallel combinations of switches, Switch level Description of – primitive gates, Simple combinational logics, simple sequential circuits, Bidirectional switches.

UNIT – V

Procedures, Tasks, Functions and Verification:

Mixed type descriptions, Procedures and Tasks: Procedures (VHDL), Tasks (Verilog),Examples of Procedures and Tasks, Functions in VHDL & Verilog HDL.

Verification: Introduction to verification, simulation, static timing Analysis, Associationlanguages and formal verification.

GATE

Not Apllicable

IES

Not Apllicable

5. List of Expert Details:

- Dr. Shaik Rafi Ahamed, Dept. of EEE, IIT Guwahati
  Phone: +91-361-2582542, Email: rafiahamed@iitg.ac.in
- Prof. V. Janakiraman, Dept. of EE, IIT Madras
  Phone: +91-44-22574485, Email: janakiraman@ee.iitm.ac.in
- Dr. Cyril Prasanna Raj, Prof. & Dean, MS Engineering College, Bangalore
  Email: cyril@msec.ac.in
- Dr. Hanho Lee, Professor School of Information and Communication Engineering, Inha University, Korea.
  Email: hhlee@inha.ac.kr

6. Journals with min 5 reference papers for literature study:

1. Routing Architecture and Applications of FPGA: A survey
https://iopscience.iop.org/article/10.1088/1742-6596/1717/1/012025/pdf

2. The Detection of Malicious Modifications in the FPGA
https://dl.acm.org/doi/abs/10.1007/s10836-022-06004-z

3. A Real-Time Image Processing with a Compact FPGA-Based Architecture

https://www.design-reuse.com/articles/10943/a-real-time-image-processing-with-a-compact-fpga-based-architecture.html

4. High Performance Programmable FPGA Overlay for Digital Signal Processing
https://link.springer.com/chapter/10.1007/978-3-642-19475-7_39

5. Efficient FPGA Implementation of an RFIR Filter Using the APC–OMS Technique with WTM for High-Throughput Signal Processing
https://www.mdpi.com/2079-9292/11/19/3118

7. Subject Lesson Plan:

Topic Name	No. of classes	Text books
UNIT I: SPLD, CPLD, FPGA		
Programmable Read Only Memories	1	T1
Programmable Logic Arrays	1	T1
Programmable Array Logic	1	T1
Masked Gate Array ASIC	1	T1
CPLD Architectures, Function Blocks	2	T1
I/O Blocks, Clock Drivers	1	T1
Interconnect CPLD Technology and Programmable Elements	1	T1
Embedded Devices	1	T1
FPGA Architectures, Configurable Logic Blocks	2	T1
Configurable I/o Blocks, Embedded Devices	1	T1
Programmable Interconnect, Clock Circuitry	2	T1
SRAM vs. Anti-fuse programming, FPGA Selection Criteria	2	T1
Total No. of Classes	**16**	
UNIT II: Universal Design Methodology for Programmable Devices		

Introduction to UDM and UDM-PD, writing a Specification	1	T1
Specification Review, ChoosingDevice and Tools	1	T1
Design, Verification, Final Review	1	T1
System Integration and Test	1	T1
Hardware Descriptive Languages, Structure of VHDL & Verilog module	1	T1, R1
Operator, Data types, Top-Down Design	2	T1, R1
Synchronous Design, Floating Nodes	1	T1, R1
Bus Contention, One-Hot state Encoding	1	T1, R1
Total No. of Classes	**09**	
UNIT III: Data flow Description and Behavioral Descriptions		
Introduction to styles types of hardware description	1	T2, R1
Behavioral, Structural, Dataflow and Mixed type and language descriptions	2	T2, R1
Structure of the dataflow description, Signal Declaration and Assignment Statements	2	T2, R1
Concurrent Signal assignments, Constant declaration and assignments	1	T2, R1
Assigning a delay time to the signal, Data type-Vectors	1	T2, R1
Structure of the HDL Behavioral description, The VHDL/ Verilog HDL variable	1	T2, R1
Assignment statement, sequential statement – IF	2	T2, R1
Signal and variable assignment, CASE & LOOP statements	2	T2, R1
Total No. of Classes	**12**	
UNIT IV: Structural and Switch level Descriptions		

Organization of the structural description, binding, state machines	1	T2, R1
Generate (HDL), Generic (VHDL), and parameter (Verilog)	2	T2, R1
Useful definitions, Single NMOS & PMOS switches	1	T2, R1
Verilog & VHDL description of NMOS & PMOS Switches	1	T2, R1
Serial and parallel combinations of switches	1	T2, R1
Switch level Description of –primitive gates,	1	T2, R1
Simple combinational logics	2	T2, R1
Simple sequential circuits, Bidirectional switches	2	T2, R1
Total No. of Classes	**11**	
UNIT V: Procedures, Tasks, Functions and Verification		
PProcedures (VHDL), Tasks (Verilog)	2	T2, R1
Examples of Procedures and Tasks	1	T2, R1
Functions in VHDL & Verilog HDL	2	T2, R1
Introduction to verification, simulation	1	T2, R1
Static timing Analysis, Association languages and formal verification	2	T2, R1
Total No. of Classes	**08**	
Total No. of Classes	**56**	

8. Suggested Books:

TEXT BOOKS:

1. Designing with FPGAS & CPLDS- Bob Zeidman, CMP Books, First Printed in India2011
2. HDL Programming Fundamental-VHDL & Verilog, Botros, Cengage Learning, ThirdIndian Reprint 2012

REFERENCE BOOKS:

1. Verilog HDL: A guide to Digital Design and Synthesis, Samir Palnitkar, Pearson

9. Websites for self learning Resources:

1. https://youtu.be/gCAYY0fHPq4
2. https://youtu.be/dQDIWFxmP2E
3. https://youtu.be/_IgaKFKg3H8
4. https://youtu.be/wANFPIPIC9Q
5. https://fpgatutorial.com
6. https://www.electronics-tutorial.net/programmable-logic-devices/complex-programmable-logic-device/
7. https://www.asic-world.com/verilog/veritut.html
8. https://nandland.com/introduction-to-vhdl-for-beginners-with-code-examples/

10. Question Banks

1.JNTUH/Model papers

11. Case study presentations:

Project 1: FPGA Implementation of AES-based Crypto Processor

Increased demand for data security is an undeniable fact. To achieve higher security, cryptographic algorithms play an essential role in protecting data from unapproved usage. In this FPGA project, we present a cryptoprocessor using Advanced Encryption Standard (AES). The AES is integrated with a 32-bit general-purpose 5- stage pipelined MIPS processor. The integrated AES module is a fully pipelined module which follows the inner round and outer round pipeline design. The results show that the presented pipeline version of the AES algorithm and the MIPS processor outperform traditional methods. At the operating frequency of 553

MHz, the proposed design can achieve the throughput of 58 Gbps, the latency of 240 ns, and the minimum power consumption of 76 MW.

This design is implemented so that crypto instructions do not block the processor's instruction fetch cycle even though the crypto co-processor is running simultaneously. By default, each instruction is fetched from the instruction memory unit and completed all its cycles on the MIPS processor if the instruction is designed for the processor. However, if the fetch instruction is not a MIPS instruction, it will be sent to the crypto co-processor in the next clock cycle after the decode stage. Crypto co-processors with MIPS are incorporated and make this integration so that crypto co-processors run by the MIPS without disturbing pipeline stages. The main contributions of this project are as follows:

- The pipeline version of AES is implemented, obtaining high throughput, low latency, and low power consumption.
- The integration of AES and MIPS is presented, which can run at different frequencies.
- The implemented AES acts as a cryptoprocessor controlled by MIPS instruction while it does not disturb the MIPS processor's pipeline stages.

Project 2: AXI4-Stream Protocol Interface on FPGA

Advanced eXtensible Interface 4 (AXI4) is a bus family established as part of the ARM Advanced Microcontroller Bus Architecture (AMBA) standard of the fourth generation. In 1996, AXI was first implemented in the third generation of AMBA, such as AXI3.

The AMBA specification specifies 3 AXI4 protocols:

AXI4: A data and address interface mapped to a high-performance memory. Capable of Burst access on devices mapped to memory.

AXI4-Lite: A subset of AXI that lacks the potential for the burst access. It has an implementation that is easier than the full AXI4 interface.

AXI4-Stream: A fast unidirectional master-to-slave data transfer protocol.

Xilinx Vivado helps with AXI4 interfaces to build a custom IP. You may connect these devices to the Zynq Processing System or other devices. The AXI4-Lite interface process will be protected by this project, which is useful for implementing memory mapping registers. There are two global signals for any AXI component: the clock ACLK and an active-low asynchronous reset ARESETN. On the rising edge of the clock, all AXI4 signals are sampled, and all signal alterations must occur after the rising edge. For the transfer of address, data, and control information, all five transaction channels use the same VALID/READY handshake method. This two-way flow control mechanism means that both the master and the slave can control the rate at which the master and the slave move the data. The information source produces a VALID signal to indicate when the address, data or control information is available. The information destination produces the READY signal to indicate that it can accept the information. When all True and READY signals in a channel are asserted during a rising clock edge, the handshake completes.

12. Assignment Questions:

SET 1

1. Explian about PAL with Example?

2. Explain Anti-fuse Programming in FPGa's?

3. Explain the architecture of FPGA's with neat sketches?

4. Explain about structure of VHDL & Verilog module operator?

5. Explain briefly about Masked gate arrays?(CO1)

6.Explain Anti-fuse Programming in FPGa's?(CO1)

7.Decribe briefly about UDM?(CO2)

8.Explain about structure of VHDL & Verilog module operator?(CO2)

SET 2

1. Explian about PAL with Example?

2. Explain with neat sketches CPLD architecture?

3.Explain the architecture of FPGA's with neat sketches?

4.Explain Top down design approach?

5. a)Explian about assignment statement with example?

b)Explain about sequential statement with example?

6. a)Explian about CASE statement with example?

b) Explain about Loop statement with example?

7.a) Expalin about Generate with example?

b)Explain aboput parameter with example?

8.a)Write the switch level description of cmos inverter?

b)Explain about Procedures and tasks with example?

SET 3

1. a)Explian about assignment statement with example?

b)Explain about sequential statement with example?

2.a) Write the switch level decription of cmos AND gate?

b)write the switch level description D-latch?

3.a)Explain the Data type vectors?

b)Explain the signal declaration and assignment statements?

4.a)Define the term "simulation"?

b)Explain the functions in verilog and vhdl?

5. a)Explian about assignment statement with example?

b)Explain about sequential statement with example?

6. a) Write the switch level decription of cmos OR gate?

b) Write the switch level description 2*1 multiplexer?

7.a)Explain the Data type vectors?

b)Explain the signal declaration and assignment statements?

8.a)Define the term "simulation"?

b)Explain the functions in verilog and vhdl?

13. List of Topics for student seminars

1. Anti fuse Programming in FPGAs
2. One Hot state encoding
3. FPGA Robotic Applications
4. Clock circuitry
5. Masked gate array ASIC
6. Synthesizable Verilog Coding
7. FPGA Switches and Routers
8. Verilog Tutorial
9. VHDL Tutorial
10. Image Processing using FPGA's

14.STEP/Course material in softcopy

FPGA PROGRAMMING NOTES.rar

15.Expert Lectures with topics & Schedules

Expert Name	Topic	Schedule (Tentative)
Dr. B. Rajendra Naik	FPGA Architeture	20/02/2023
Dr. N. Srikanth	VHDL & Verilog Programming	13/03/2023

ACADEMIC PLANNER

For

"OBJECT ORIENTED PROGRAMMING THROUGH JAVA"

Presented by

M.PRABHAKAR

Department of
Computer Science and Engineering

CMR ENGINEERING COLLEGE
(Approved by AICTE-NewDelhi, Affiliated to J.N.T.U, Hyderabad)
Kandlakoya(v),Medchal Road,Hyderabad-501 401,Telangana State, India .Website: www.cmrec.ac.in
(AY:2021-22)

ACADEMIC PLANNER

Subject: Object Oriented Programming through Java

S.NO		CONTENT
(1)	**-**	**Preamble/Introduction**
(2)	**-**	**Prerequisites**
(3)	**-**	**Objectives and Outcomes**
(4)	**-**	**Syllabus** **1.R18-JNTUH** **2.GATE** **3.IES**
(5)	**-**	**List of Expert Details**(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6)	**-**	**Journals with min 5 ref paper for literature study**
(7)	**-**	**Subject -Lesson plan**
(8)	**-**	**Suggested Books (**Prescribed and References)
(9)	**-**	**Websites for self-learning resources like** *www.geeksforgeeks.org, www.schools.com, Coursera, edX, Udemy, Khan Academy*, NPTEL etc along Registration procedures*)*
(10)	**-**	**Question Banks** **1.JNTUH/Model papers** **2.GATE**
(11)	**-**	**Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications.**
(12)	**-**	**Assignment Question/Innovative Assignments sets.**
(13)	**-**	**List of topics for students Seminars with Guidelines**
(14)	**-**	**STEP/Course material in softcopy**
(15)	**-**	**Expert Lectures with topics &Schedules(if any)**

1. Preamble/Introduction:

Java is a **programming** language created by James Gosling from Sun Microsystems (Sun) in 1991. The target of **Java** is to write a program once and then run this program on multiple operating systems. The first publicly available version of **Java** (**Java** 1.0) was released in 1995.

2. **PREREQUISITES:**

To learn Java, you must have the basic knowledge of C programming language.

3. OBJECTIVES & OUTCOMES

1. Objectives

- To introduce object oriented programming concepts.
- To understand of OOP Concept and apply them in solving problems
- To introduces the concept of Inheritance, Polymorphism and Abstract classes
- Implementation of Packages and Interfaces
- Implementation of Exception Handling and Multithreading
- The concept of GUI Applications, Swings, and Applets

2. Outcomes

- Able to solve real world problems using OOP techniques.
- Able to understand the use of abstract classes.
- Able to solve problems using java collection framework and I/O classes.
- Able to develop multithreaded applications with synchronization.
- Able to develop applets for web applications.
- Able to design GUI based applications

4. SYLLABUS

4.1 JNTU Hyderabad Syllabus

Unit – 1

Object-Oriented Thinking- A way of viewing world – Agents and Communities, messages and methods, Responsibilities, Classes and Instances, Class Hierarchies- Inheritance, Method binding, Overriding and Exceptions, Summary of Object-Oriented concepts. Java buzzwords, An Overview of Java, Data types, Variables and Arrays, operators, expressions, control statements, Introducing classes, Methods and Classes, String handling.

Inheritance– Inheritance concept, Inheritance basics, Member access, Constructors, Creating Multilevel hierarchy, super uses, using final with inheritance, Polymorphism-ad hoc polymorphism, pure polymorphism, method overriding, abstract classes, Object class, forms of inheritance-specialization, specification, construction, extension, limitation, combination, benefits of inheritance, costs of inheritance.

Unit – 2

Packages- Defining a Package, CLASSPATH, Access protection, importing packages.
Interfaces- defining an interface, implementing interfaces, Nested interfaces, applying interfaces, variables in interfaces and extending interfaces.
Stream based I/O (java.io) – The Stream classes-Byte streams and Character streams, Reading console Input and Writing Console Output, File class, Reading and writing Files, Random access file operations, The Console class, Serialization, Enumerations, auto boxing, generics.

Unit – 3
Exception handling - Fundamentals of exception handling, Exception types, Termination or resumptive models, Uncaught exceptions, using try and catch, multiple catch clauses, nested try statements, throw, throws and finally, built-in exceptions, creating own exception sub classes.
Multithreading- Differences between thread-based multitasking and process-based multitasking, Java thread model, creating threads, thread priorities, synchronizing threads, inter thread communication.

Unit – 4
The Collections Framework (java.util)- Collections overview, Collection Interfaces, The Collection classes- Array List, Linked List, Hash Set, Tree Set, Priority Queue, Array Deque. Accessing a Collection via an Iterator, Using an Iterator, The For-Each alternative, Map Interfaces and Classes, Comparators, Collection algorithms, Arrays,. The Legacy Classes and Interfaces- Dictionary, Hashtable ,Properties, Stack, Vector More Utility classes, String Tokenizer, Bit Set, Date, Calendar, Random, Formatter, Scanner

Unit - 5
GUI Programming with Swing – Introduction, limitations of AWT, MVC architecture, components, containers. Understanding Layout Managers, Flow Layout, Border Layout, Grid Layout, Card Layout, Grid Bag Layout.
Event Handling- The Delegation event model- Events, Event sources, Event Listeners, Event classes, Handling mouse and keyboard events, Adapter classes, Inner classes, Anonymous Inner classes.
A Simple Swing Application, Applets – Applets and HTML, Security Issues, Applets and Applications, passing parameters to applets. Creating a Swing Applet, Painting in Swing, A Paint example, Exploring Swing Controls-JLabel and Image Icon, JText Field, **The Swing Buttons**- JButton, JToggle

Button, JCheck Box, JRadio Button, JTabbed Pane, JScroll Pane, JList, JCombo Box, Swing Menus, Dialogs.

4.2 GATE Syllabus

Basics of Programming – Recursion, Array, Strings, Exception Handling, Collection Framework.

5. EXPERT DETAILS

- **International**

  James Gosling

  Engineer at Amazon Web Services (AWS) and the original developer of Java,
  Blog: **nighthacks.com/roller/jag**

- **National**

  Mr. Ranganath Vadapalli,

  Java full stack developer, JP Morgan Chase, Email - vadapalliranganath@gmail.com,

  Contact No – 8884057329, Expert in Java, java8, Spring Boot, Angular and React JS.

- **Local**

  Dr. Vignesh Janarthanan

  Professor, HOD, Department of CSE, Malla Reddy Institute of Technology and Science Contact No-8106193443, Email id: vigneshj2004@gmail.com

6. JOURNALS

a. An interactive environment for beginning Java programmers
b. PAMELA: An annotation-based Java modeling framework - ScienceDirect
c. A type-directed algorithm to generate random well-typed Java 8 programs - ScienceDirect

d. Concept–based Analysis of Java Programming Errors among Low, Average and High Achieving Novice Programmers

e. Java Tutorial, Java EE Tutorials - JournalDev

7. Subject Lesson Plan

S.NO	Topic (syllabus)	Sub-Topic	NO. OF LECTURES REQUIRED	Suggested Books	Teaching Methods
1	**Unit – 1**				
2	**Object-Oriented Thinking**	Agents and Communities, messages and methods, and Responsibilities	1	T1, T2	BB / PPT
5		Classes and Instances, Class Hierarchies		T1, T2	BB / PPT
7		Inheritance, Method binding	1	T1, T2	BB / PPT
9		Overriding and Exceptions		T1, T2	BB / PPT
10		Summary of Object-Oriented concepts	1	T1, T2	BB / PPT
11		Java buzzwords	1	T1, T2	BB / PPT
12		An Overview of Java		T1, T2	BB / PPT
13		Data types, Variables and Arrays	1	T1, T2	BB / PPT
15		operators, expressions	1	T1, T2	BB / PPT
17		control statements	1	T1, T2	BB / PPT
18		Introducing classes, Methods and Classes	1	T1, T2	BB / PPT
20		String handling	1	T1, T2	BB / PPT
21	**Inheritance**	Inheritance concept, Inheritance	1	T1, T2	BB / PPT

		basics			
23		Member access, Constructors	1	T1, T2	BB / PPT
25		Creating Multilevel hierarchy	1	T1, T2	BB / PPT
26		super uses, using final with inheritance	1	T1, T2	BB / PPT
28		Polymorphism-ad hoc polymorphism	1	T1, T2	BB / PPT
29		pure polymorphism	1	T1, T2	BB / PPT
30		method overriding, abstract classes, Object class	1	T1, T2	BB / PPT
33		forms of inheritance- specialization, specification, construction, extension, limitation, combination	1	T1, T2	BB / PPT
34		benefits of inheritance and costs of inheritance		T1, T2	BB / PPT
36		**Total classes required for UNIT - 1**	17		
37	**UNIT – 2**				
38	**Packages**	Defining a Package	1	T1, T2	BB / PPT
39		CLASSPATH		T1, T2	BB / PPT
40		Access protection		T1, T2	BB / PPT
41		importing packages	1	T1, T2	BB / PPT
42	**Interfaces**	defining an interface		T1, T2	BB / PPT
43		implementing interfaces	1	T1, T2	BB / PPT
44		Nested interfaces		T1, T2	BB / PPT
45		applying interfaces	1	T1, T2	BB / PPT
46		variables in interfaces		T1, T2	BB / PPT
47		extending interfaces		T1, T2	BB / PPT
48	**Stream based I/O**	classes-Byte streams and Character streams	1	T1, T2	BB / PPT

49		Reading console Input and Writing Console Output		T1, T2	BB / PPT
50		File class	1	T1, T2	BB / PPT
51		Reading and writing Files		T1, T2	BB / PPT
52		Random access file operations	1	T1, T2	BB / PPT
53		The Console class		T1, T2	BB / PPT
54		Serialization	1	T1, T2	BB / PPT
55		Enumerations	1	T1, T2	BB / PPT
56		auto boxing		T1, T2	BB / PPT
57		generics		T1, T2	BB / PPT
58		**Total classes required for UNIT - 2**	9		
59	**UNIT – 3**				
60	**Exception handling**	Fundamentals of exception handling	1	T1, T2	BB / PPT
61		Exception types		T1, T2	BB / PPT
62		Termination or resumptive models	1	T1, T2	BB / PPT
63		Uncaught exceptions		T1, T2	BB / PPT
64		using try and catch	1	T1, T2	BB / PPT
65		multiple catch clauses		T1, T2	BB / PPT
66		nested try statements	1	T1, T2	BB / PPT
67		throw, throws and finally		T1, T2	BB / PPT
68		built- in exceptions	1	T1, T2	BB / PPT
69		creating own exception sub classes	1	T1, T2	BB / PPT
70	**Multithreading**	Differences between thread-based multitasking and process-based multitasking	1	T1, T2	BB / PPT
71		Java thread model		T1, T2	BB / PPT
72		creating threads	1	T1, T2	BB / PPT

73		thread priorities	1	T1, T2	BB / PPT
74		synchronizing threads		T1, T2	BB / PPT
75		inter thread communication	1	T1, T2	BB / PPT
76		**Total classes required for UNIT - 3**	10		
77	**UNIT – 4**				
78	**The Collections Framework**	Collections overview	1	T1, T2	BB / PPT
79		Collection Interfaces		T1, T2	BB / PPT
80		The Collection classes- Array List, Linked List, Hash Set, Tree Set, Priority Queue, Array Deque	2	T1, T2	BB / PPT
81		Accessing a Collection via an Iterator	1	T1, T2	BB / PPT
82		Using an Iterator		T1, T2	BB / PPT
83		The For-Each alternative		T1, T2	BB / PPT
84		Map Interfaces and Classes	1	T1, T2	BB / PPT
85		Comparators		T1, T2	BB / PPT
86		Collection algorithms		T1, T2	BB / PPT
87		Arrays		T1, T2	BB / PPT
88		The Legacy Classes and Interfaces- Dictionary, Hashtable ,Properties, Stack, Vector More Utility classes, String Tokenizer, Bit Set, Date, Calendar, Random, Formatter, Scanner	3	T1, T2	BB / PPT
89		**Total classes required for UNIT - 4**	8		
90	**UNIT – 5**				
91	**GUI Programming with Swing**	Introduction and limitations of AWT	1	T1, T2	BB / PPT

92		MVC architecture		T1, T2	BB / PPT
93		components	1	T1, T2	BB / PPT
94		containers		T1, T2	BB / PPT
95		Understanding Layout Managers, Flow Layout, Border Layout, Grid Layout, Card Layout, Grid Bag Layout	1	T1, T2	BB / PPT
96	**Event Handling**	The Delegation event model	1	T1, T2	BB / PPT
97		Events, Event sources, Event Listeners, and Event classes		T1, T2	BB / PPT
98		Handling mouse and keyboard events	1	T1, T2	BB / PPT
99		Adapter classes	1	T1, T2	BB / PPT
100		Inner classes		T1, T2	BB / PPT
101		Anonymous Inner classes		T1, T2	BB / PPT
102	**A Simple Swing Application, Applets**	Applets and HTML	1	T1, T2	BB / PPT
103		Security Issues		T1, T2	BB / PPT
104		Applets and Applications		T1, T2	BB / PPT
105		passing parameters to applets	1	T1, T2	BB / PPT
106		Creating a Swing Applet		T1, T2	BB / PPT
107		Painting in Swing		T1, T2	BB / PPT
108		A Paint example	1	T1, T2	BB / PPT
109		Exploring Swing Controls- JLabel and Image Icon, JText Field		T1, T2	BB / PPT
110	**The Swing Buttons**	JButton	2	T1, T2	BB / PPT
111		JToggle Button		T1, T2	BB / PPT
112		JCheck Box		T1, T2	BB / PPT
113		JRadio Button		T1, T2	BB / PPT

114		JTabbed Pane		T1, T2	BB / PPT
115		JScroll Pane		T1, T2	BB / PPT
116		JList		T1, T2	BB / PPT
117		JCombo Box		T1, T2	BB / PPT
118		Swing Menus		T1, T2	BB / PPT
119		Dialogs		T1, T2	BB / PPT
120		**Total classes required for UNIT - 5**	11		
121		**Total classes required**	**55**		

8. SUGGESTED BOOKS

Text Books

1. Java The complete reference, 9th edition, Herbert Schildt, McGraw Hill Education (India) Pvt. Ltd.[T1]
2. Understanding Object-Oriented Programming with Java, updated edition, T. Budd, Pearson Education. [T2]

Reference Books

1. An Introduction to programming and OO design using Java, J. Nino and F.A. Hosch, John Wiley & sons [R1]
2. Introduction to Java programming, Y. Daniel Liang, Pearson Education. [R2]
3. Object Oriented Programming through Java, P. Radha Krishna, University Press. [R3]
4. Programming in Java, S. Malhotra, S. Chudhary, 2nd edition, Oxford Univ. Press. [R4]
5. Java Programming and Object-oriented Application Development, R. A. Johnson, Cengage Learning. [R5]

9. WEBSITES

a. https://nptel.ac.in/courses/106/105/106105191/

b. http://www.btechsmartclass.com/java/java-tutorials.html

c. https://www.tutorialspoint.com/java/index.htm

d. https://www.w3schools.com/java/default.asp

e. https://www.programiz.com/java-programming

f. https://www.guru99.com/java-tutorial.html

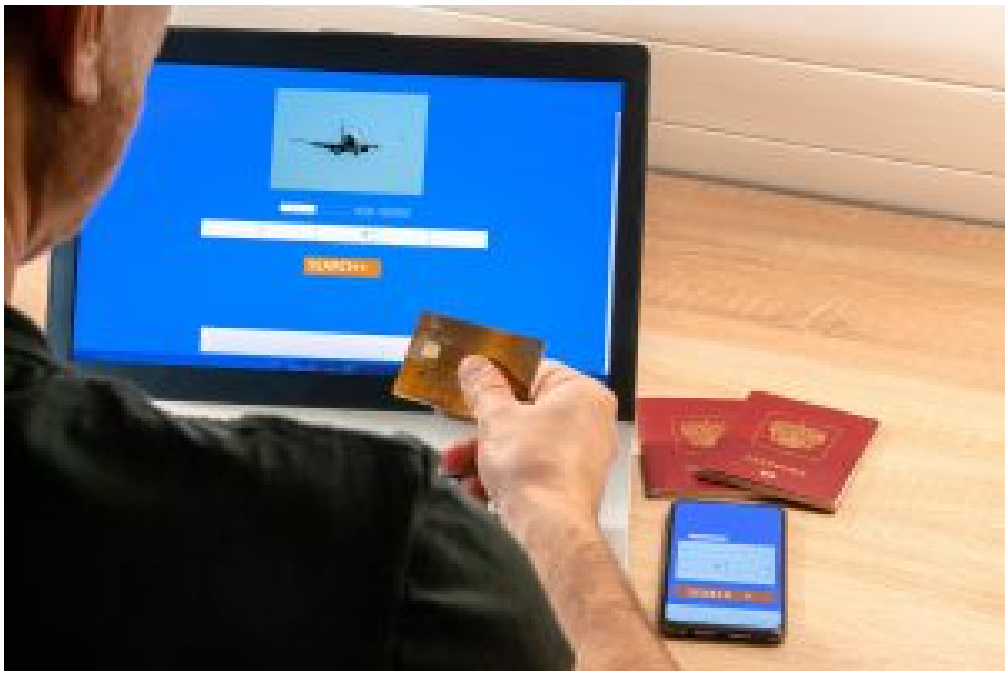
g. https://www.javatpoint.com/java-basics

10. QUESTION BANKS

JNTUH Model Papers.rar

11. CASE STUDY

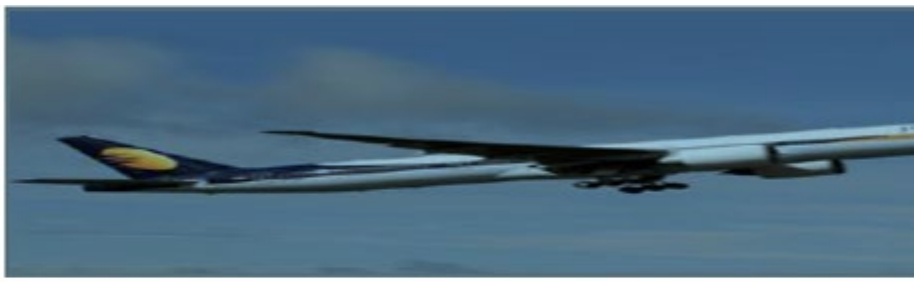
Airlines Reservation System



The airline reservation system is comprehensive passenger processing system that includes inventory, fares, e-ticket operations, and online transactions. The main features of the airline reservation system are:

- Reservation and cancellation of the airline tickets.
- Automation of airline system functions.
- Perform transaction management and routing functions.
- Offer quick responses to customers.
- Maintain passenger records and report on the daily business transactions.

This integrated airline reservation management application features an open architecture that encourages the addition of new systems and functionalities. This means that the app can be tweaked to keep up with the dynamic needs of the airline business.



WELCOME TO ONLINE RESERVATION SYSTEM

Registered Users

USERNAME
PASSWORD

REGISTRATION OFFERS CONTACT US

PLEASE FIRST REGISTER

First Name: Middle Name: Last Name:

Username:

Password:

Address:

Email:

12. ASSIGNMENT AND INNOVATIVE ASSIGNMENT QUESTIONS

- **SAMPLE ASSIGNMENT-1**

1. What is meant by byte code? Briefly explain how Java is platform independent?
2. Explain the significance of public, protected and private access specifiers in inheritance.
3. Write the significance of Java Virtual Machine.
4. How do we implement polymorphism in JAVA? Explain briefly.
5. How to design and implement an interface in java? Give an example.

- **SAMPLE ASSIGNMENT-2**

1. What is an Exception? How is an Exception handled in Java?
2. Differentiate between multiprocessing and multi-threading. What is to be done to implement these in a Program?
3. Explain the process of defining and creating a package with suitable examples.
4. What is Java Collections Framework? List out some benefits of Collections framework and explain.
5. What is an applet? Explain the life cycle of Applet with a neat sketch.

IMPORTANT QUESTION SETS OF EACH UNIT

Unit – 1

1. What is Java? Explain the features of Java.
2. Describe the Java environment
3. Explain the structure of Java program
4. Explain the data types available in Java
5. Explain type casting with example
6. Explain the scope of variable
7. List out the decision making statements available in Java. Explain with example
8. List out the looping statements available in Java. Explain with example
9. Write various types of inheritance
10. Define inheritance. Describe different forms of inheritance.

Unit – 2

1. Explain the process of defining and creating package with suitable example.
2. Describe the various forms of implementing interface. Give an example of JAVA code for each case.
3. When do we declare a method or class abstract? Discuss with one Example.
4. Write short note on method overloading and method overriding.
5. Define the term - stream, reader stream classes, writer stream classes.

Unit – 3

1. Give examples of the Run-time error
2. Explain Arithmetic Exception with an example.
3. What is exception? Explain the syntax of try block and catch block with an example.
4. Describe the try and catch statements in detail.
5. Differentiate between multiprocessing and multi-threading. What is to be done to implement these in a Program?
6. Write a program that creates two threads. First thread prints numbers from 1 to 100 and other thread prints numbers from 100 to 1.

Unit – 4

1. Discuss the differences between HashList and HashMap, Set and List?
2. What are the similarities between ArrayList and Vector? Explain.
3. What is the difference between Iterator and ListIterator? Explain different ways to iterate over a list.
4. What is Comparable and Comparator interface? Differentiate between them.

Unit – 5

1. Explain Applet life cycle in detail.
2. Write short note on following components.
   a) Label
   b) TextField
   c) TextArea
   d) List
   e) Choice
   f) Button
   g) Checkbox
3. Define (1) Event (2) Event Source (3) Event Class (4) Event Listener
4. Write difference between java applet program and java application program.
5. List down methods for KeyEvent class and ItemEvent class

13. LIST OF TOPICS FOR STUDENTS SEMINAR

- Inheritance in java
- Exception handling in java
- Interfaces in java
- Packages in java
- Collections in java
- AWT and Swings

14. **STEP MATERIAL**

JAVA PROGRAMMING_STEP_MATERIAL.rar

15. EXPERT LECTURE SCHEDULE:

Real time applications of multi-threading and swing applications – Tentative period in month of June/May 2022 first week.